

# *LA-1421 Schematics Document Ver1.0*

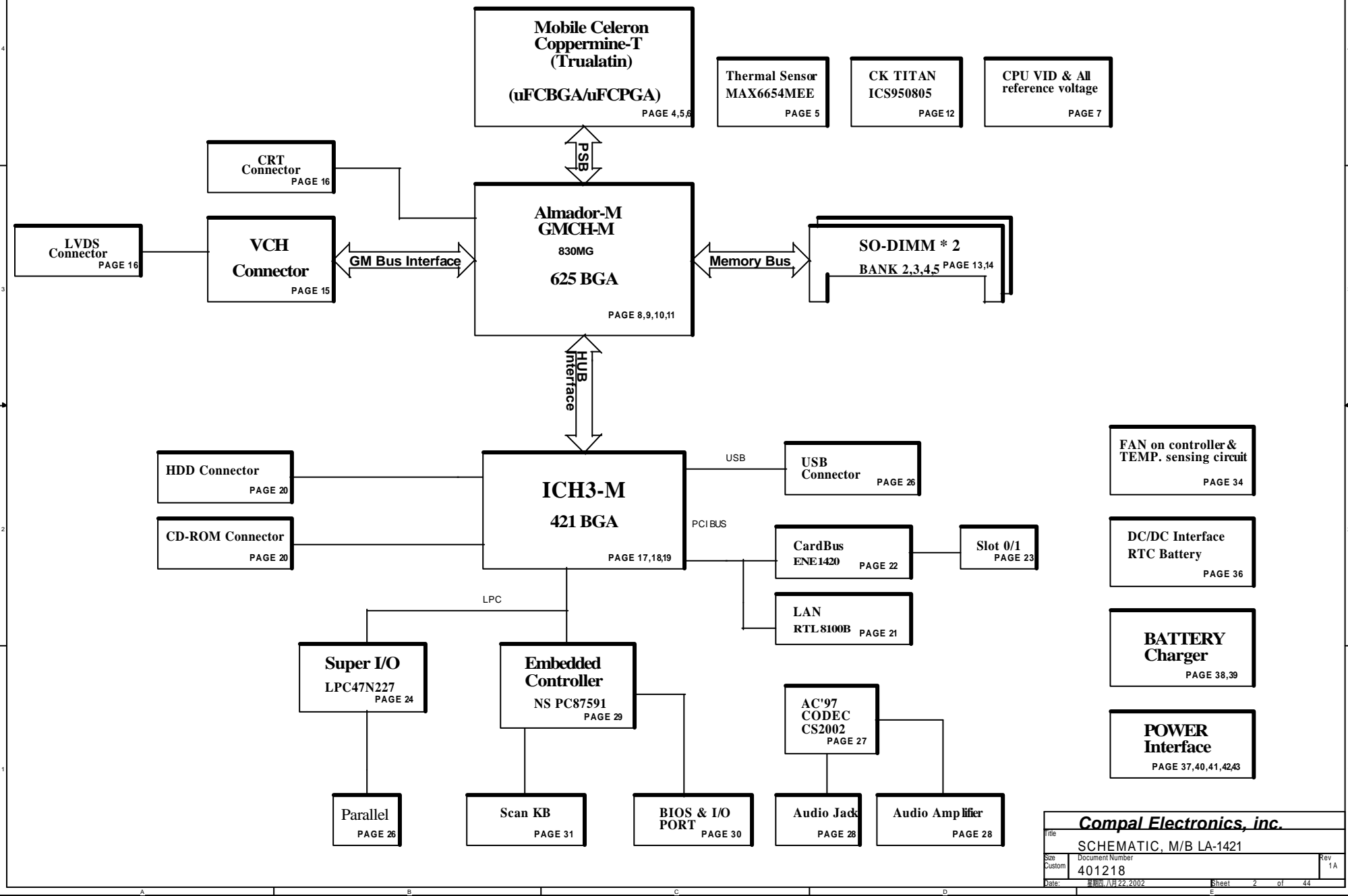
**uFCBGA/uFCPGA for Celeron/ Coppermine-T and Tualatin CPU  
Almador-M(830-MG) + ICH3 + VCH**

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# BLOCK DIAGRAM

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter powersupply(19V)	N/A	N/A	N/A
B+	AC or battery power rail for powercircuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltageforCPU	ON	OFF	OFF
+VTT	1.2V switched power railforCPUAGTLBus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
On Board LAN	AD17	3	PIRQB

## EC SM Bus1 address

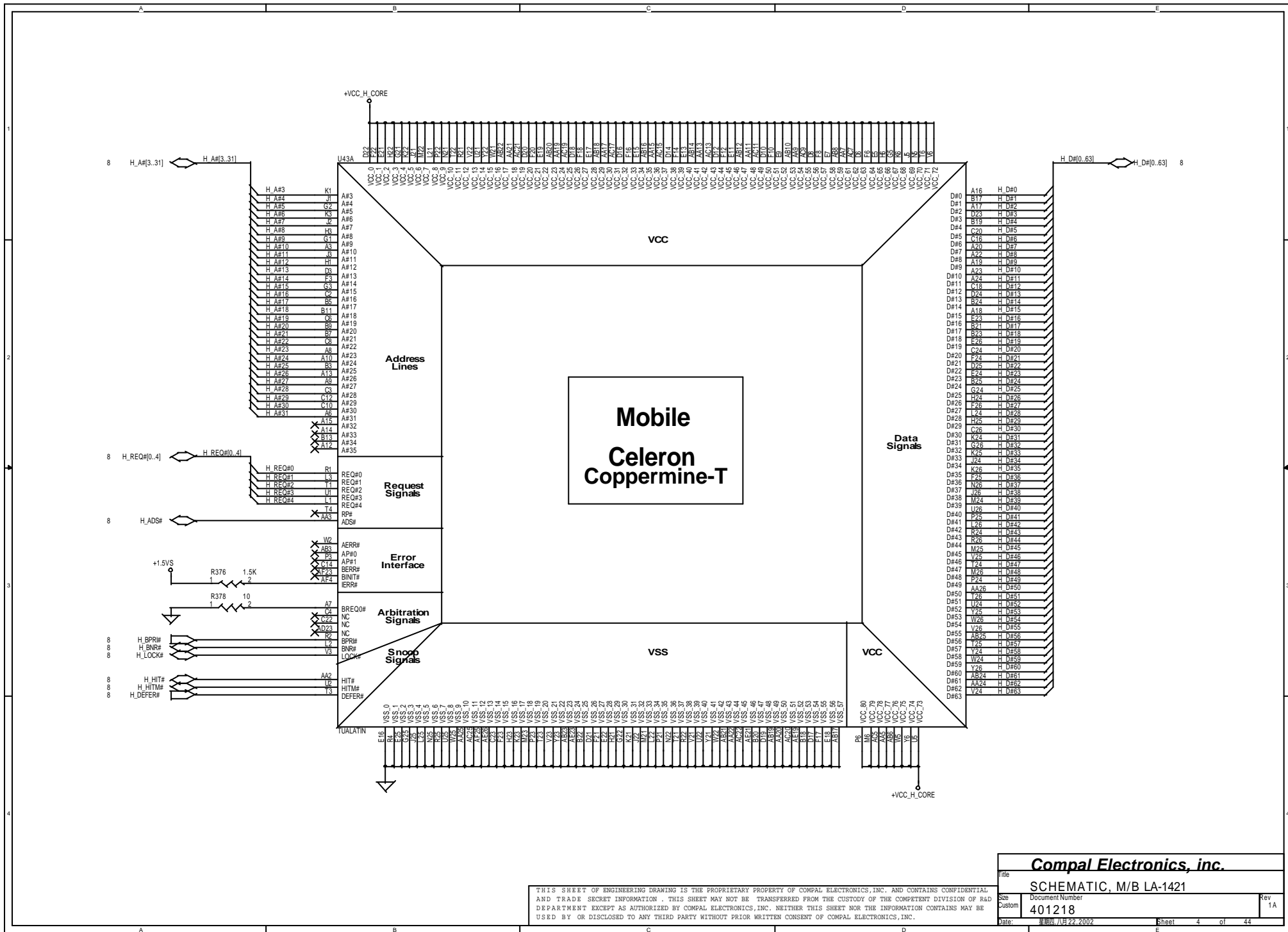
Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C1602)	1010 000X b	Smart Battery	0001 011X b
(24C04)	1011 000Xb	Docking	0011 011X b
		DOT Board	XXXX X XXXb

## EC SM Bus2 address

## ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

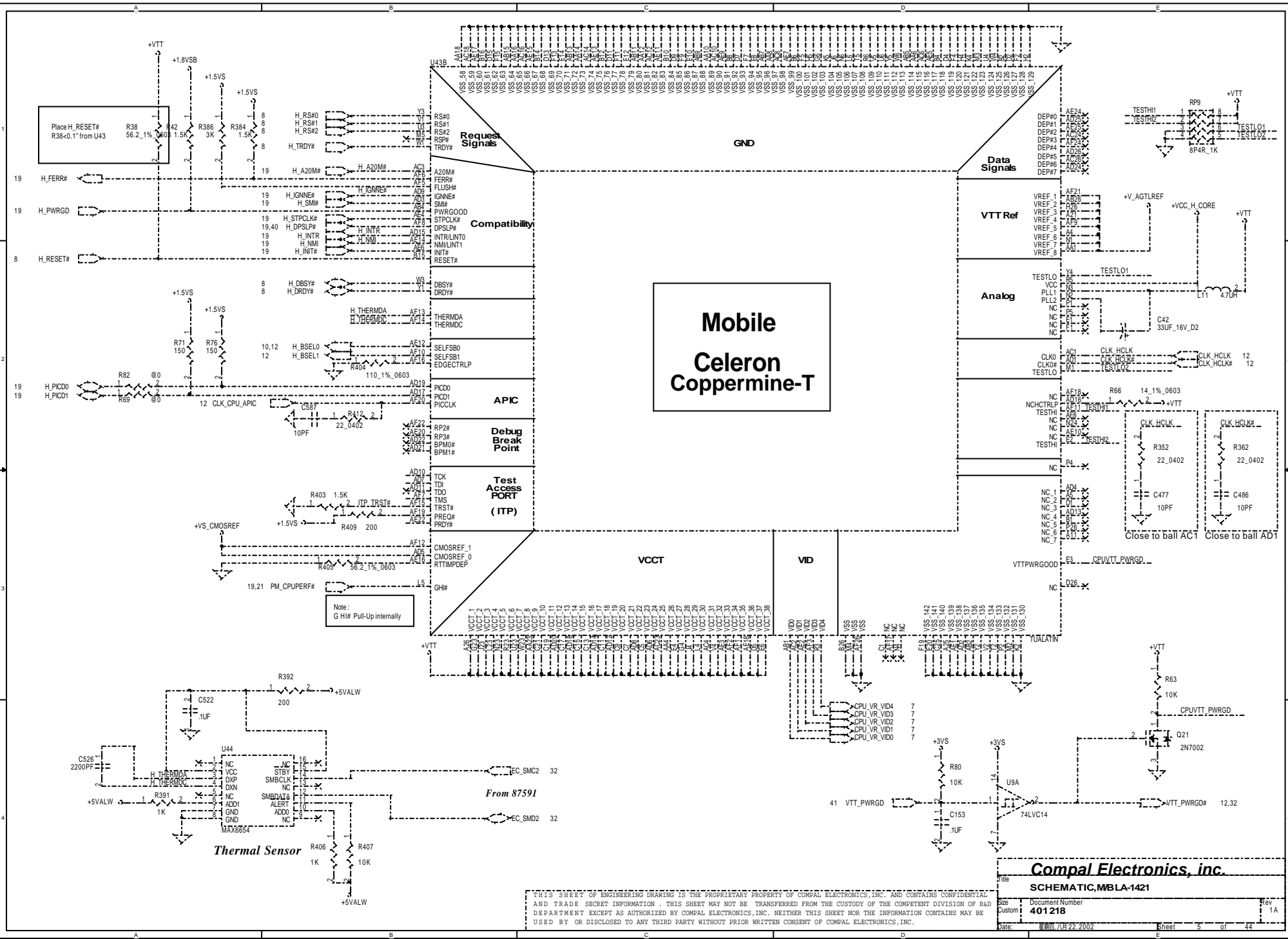
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# Mobile Celeron Coppermine-T



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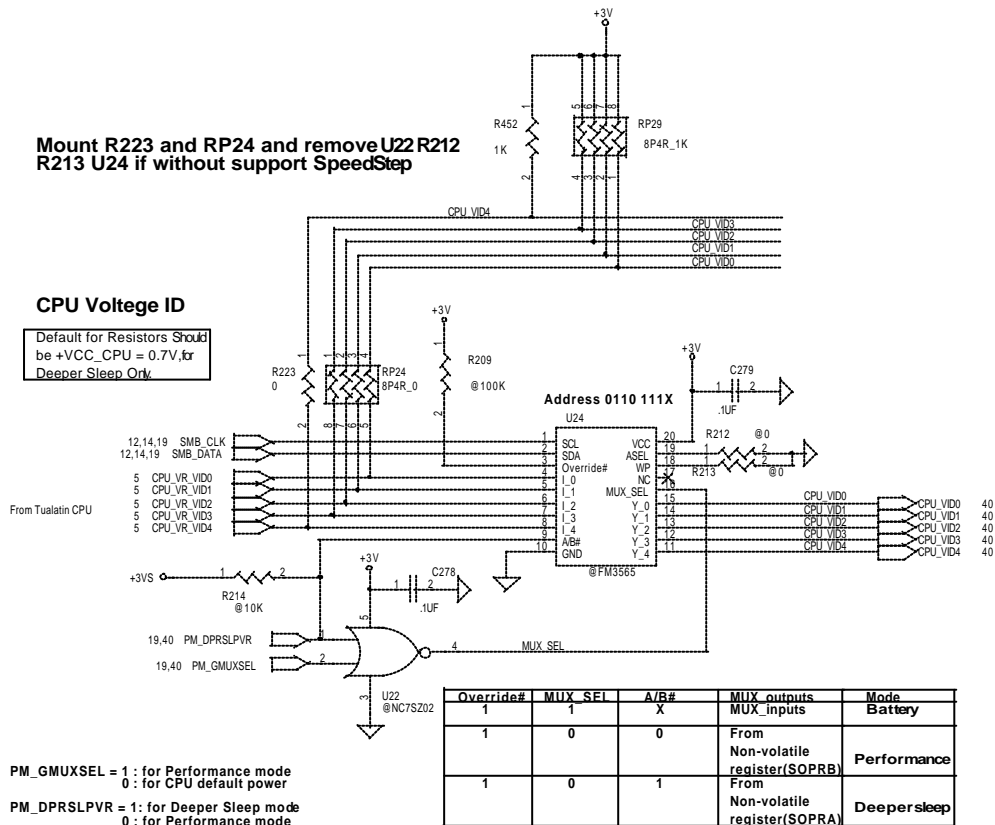
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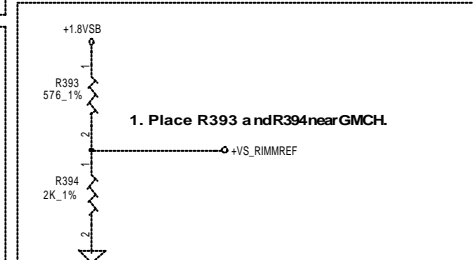
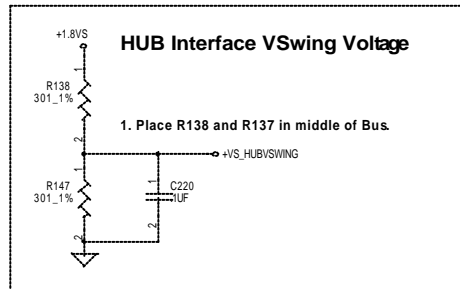
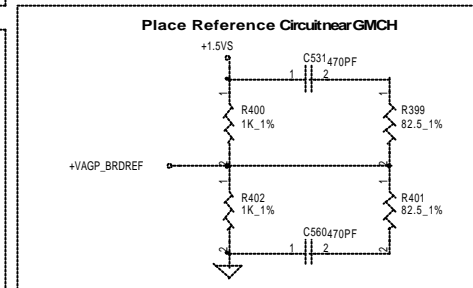
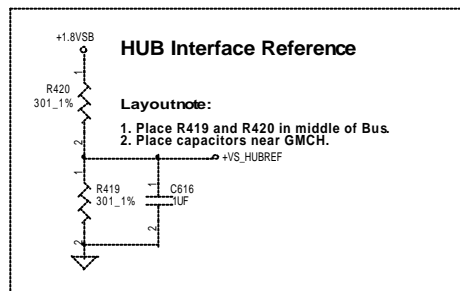
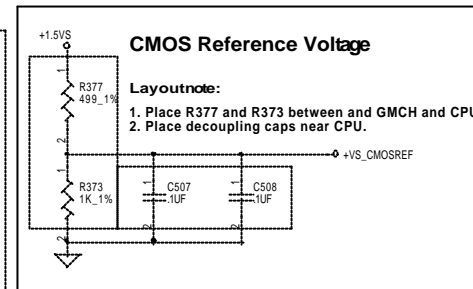
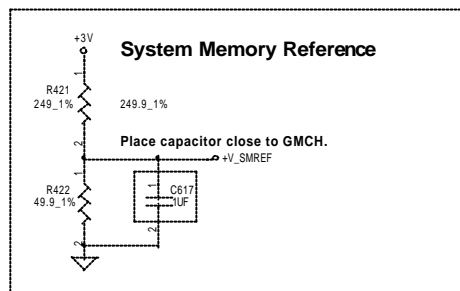
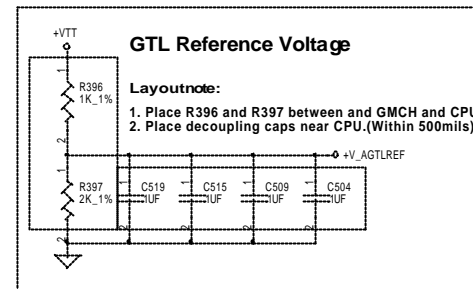
Mount R223 and RP24 and remove U22 R212 R213 U24 if without support SpeedStep

### CPU Voltage ID

Default for Resistors Should be +VCC\_CPU = 0.7V, for Deeper Sleep Only.



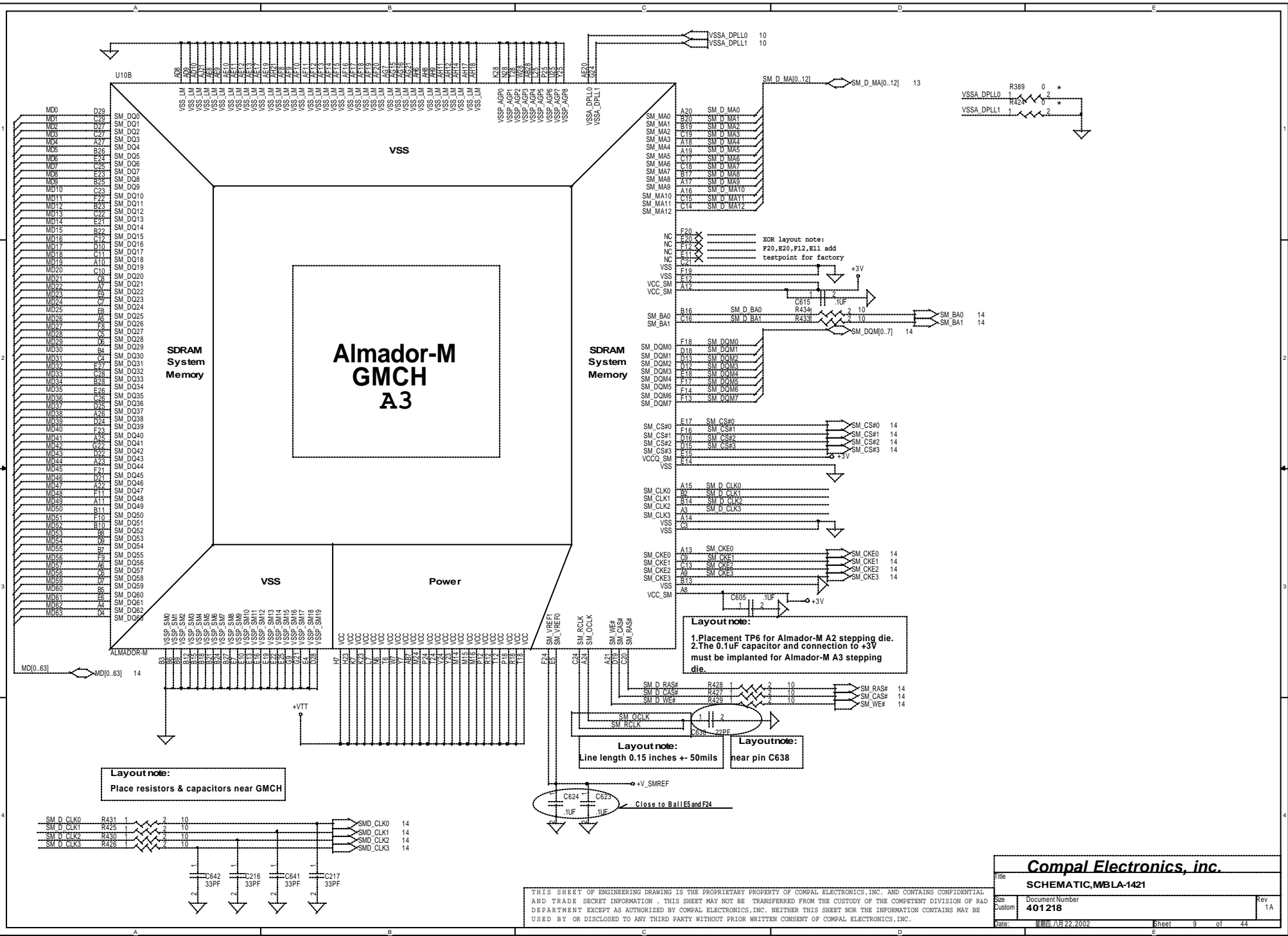
PM\_GMUXSEL = 1: for Performance mode  
0: for CPU default power  
PM\_DPRSLPVR = 1: for Deeper Sleep mode  
0: for Performance mode



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**Almador-M  
GMCH  
A3**

**SDRAM  
System  
Memory**

**SDRAM  
System  
Memory**

VSS

Power

**Layout note:**  
Place resistors & capacitors near GMCH

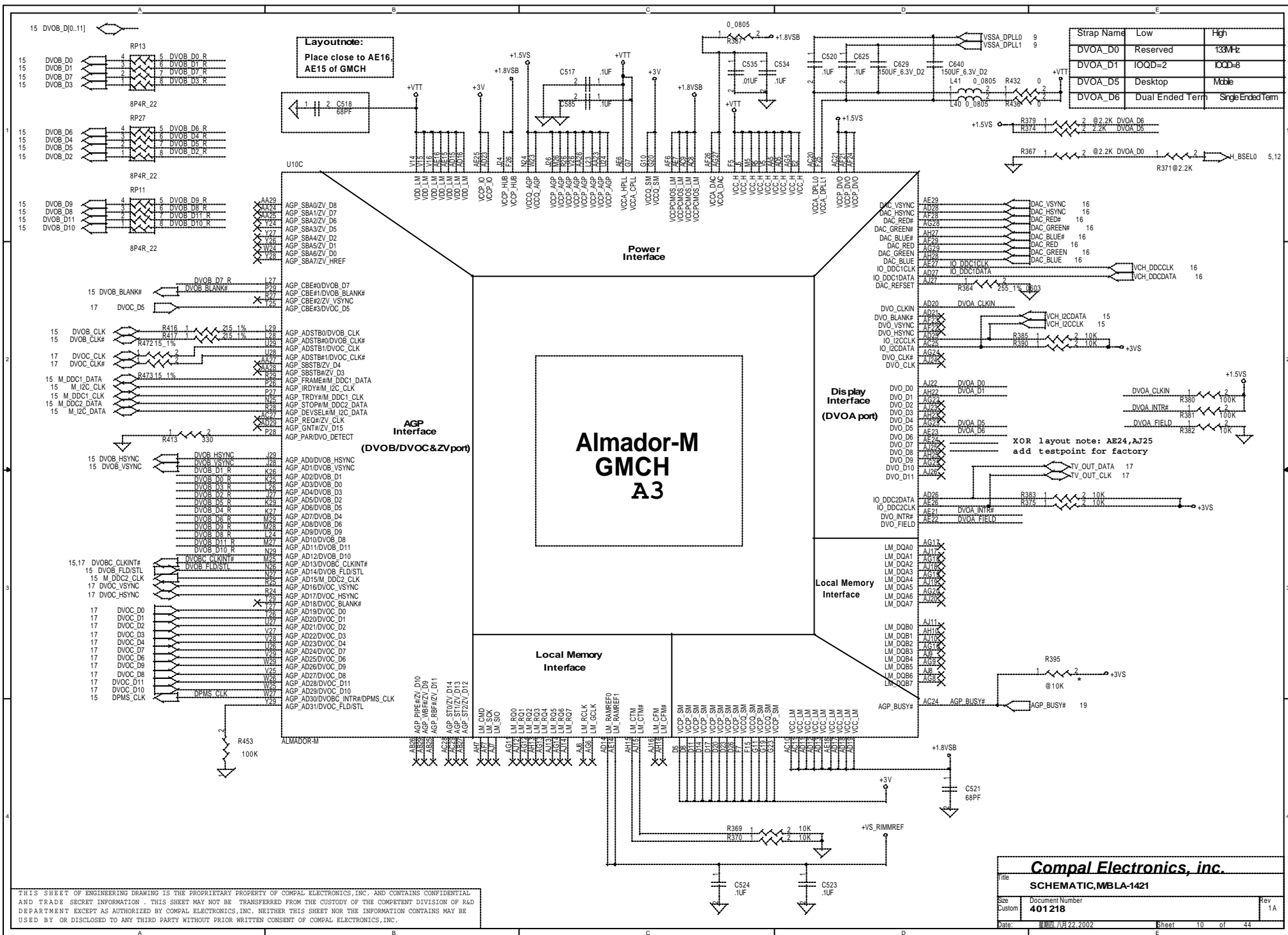
**Layout note:**  
1.Placement TP6 for Almador-M A2 stepping die.  
2.The 0.1uF capacitor and connection to +3V  
must be implanted for Almador-M A3 stepping  
die.

**Layout note:**  
Line length 0.15 inches +/- 50mils  
**Layout note:**  
near pin C638

SM_D_CLK0	R431	1	2	10	SMD_CLK0	14
SM_D_CLK1	R425	1	2	10	SMD_CLK1	14
SM_D_CLK2	R430	1	2	10	SMD_CLK2	14
SM_D_CLK3	R426	1	2	10	SMD_CLK3	14
	C642	33PF				
	C216	33PF				
	C641	33PF				
	C217	33PF				

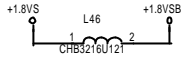
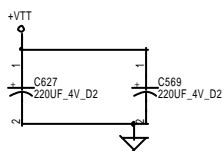
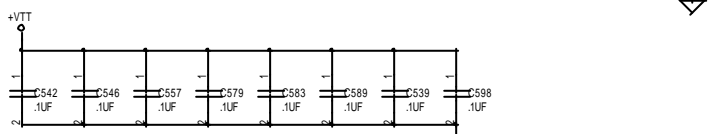
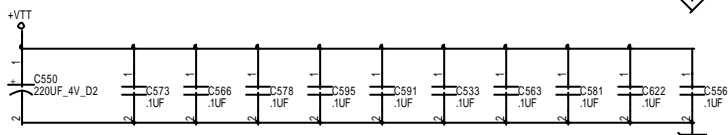
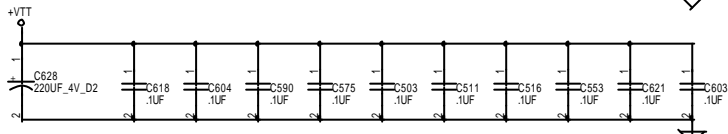
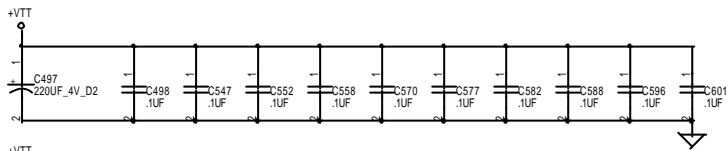
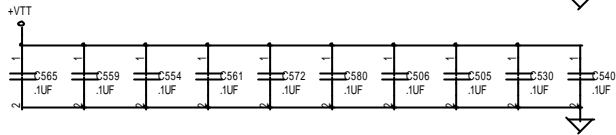
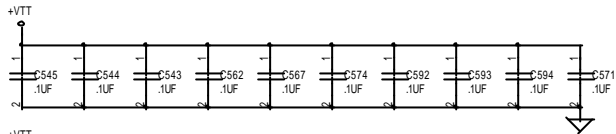
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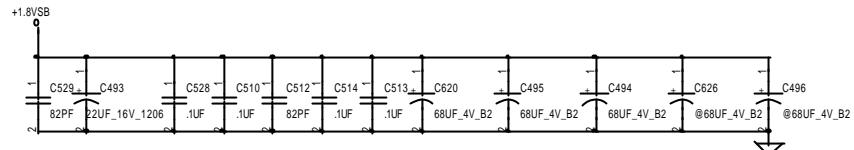


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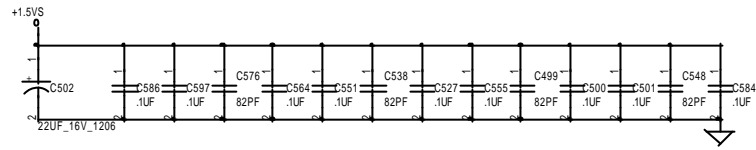
**Layout note:**  
Distribute as close as possible  
to GMCH Processor Quadrant .



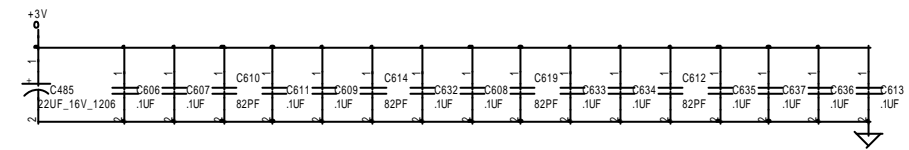
**Layout note:**  
Distribute as close as possible  
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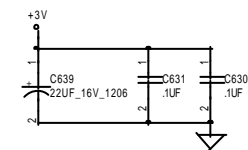
**Layout note:**  
Distribute as close as possible  
to GMCH AGP/DVO Quadrant .



**Layout note:**  
Distribute as close as possible  
to GMCH System Memory Quadrant .

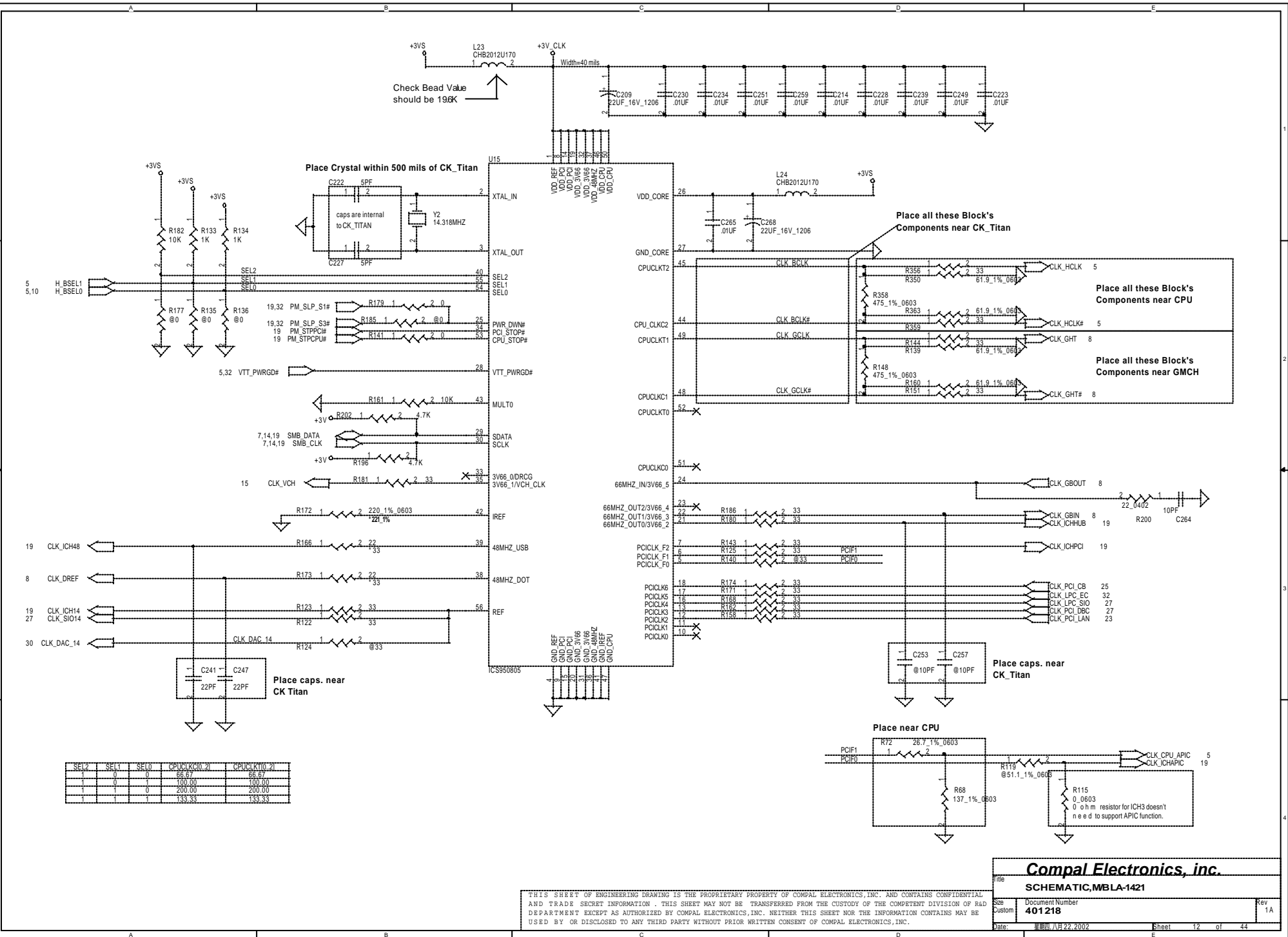


**Layout note:**  
Distribute as close as possible  
to IO Quadrant .



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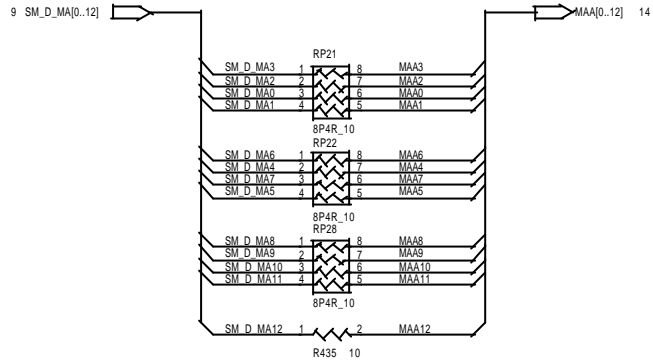
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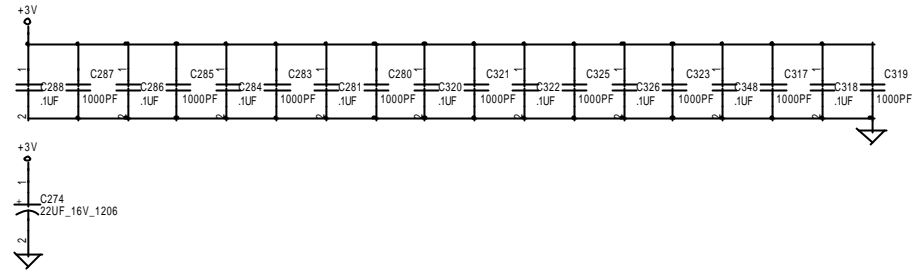
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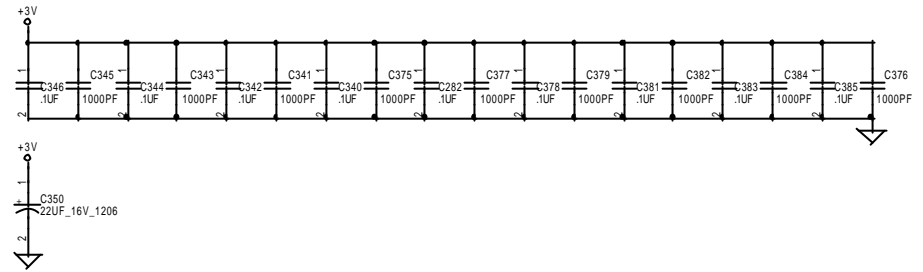
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**Layout note:**  
 One .1uF cap per power pin .  
 Place each cap close to SODIMM(DIMM 0) pin .



**Layout note:**  
 One .1uF cap per power pin .  
 Place each cap close to SODIMM(DIMM 1) pin .



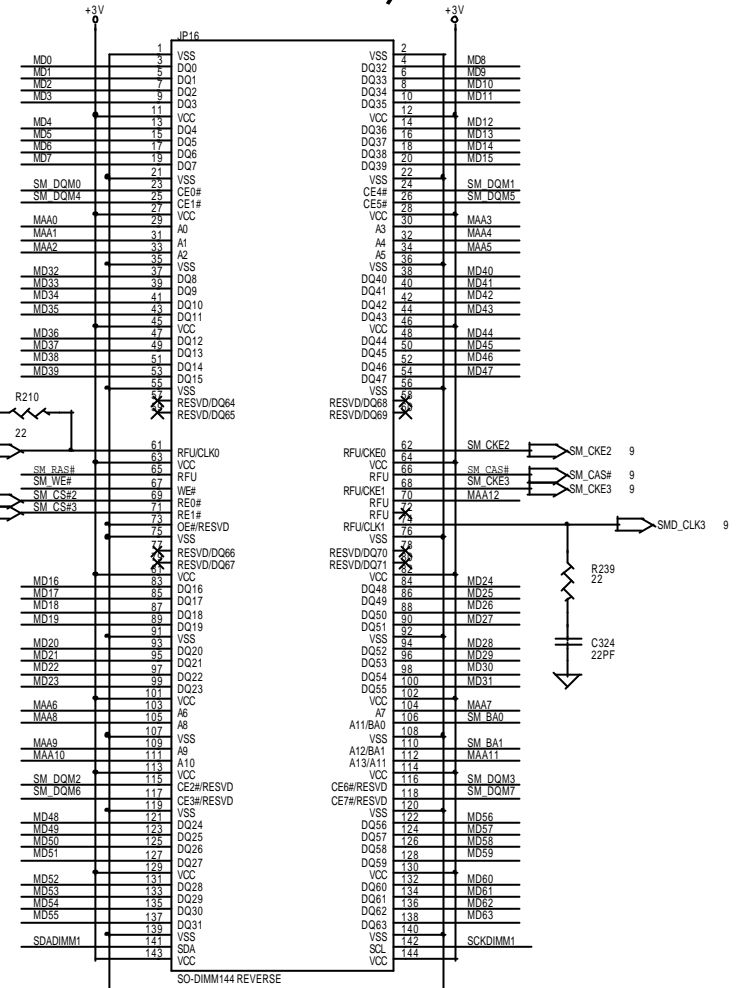
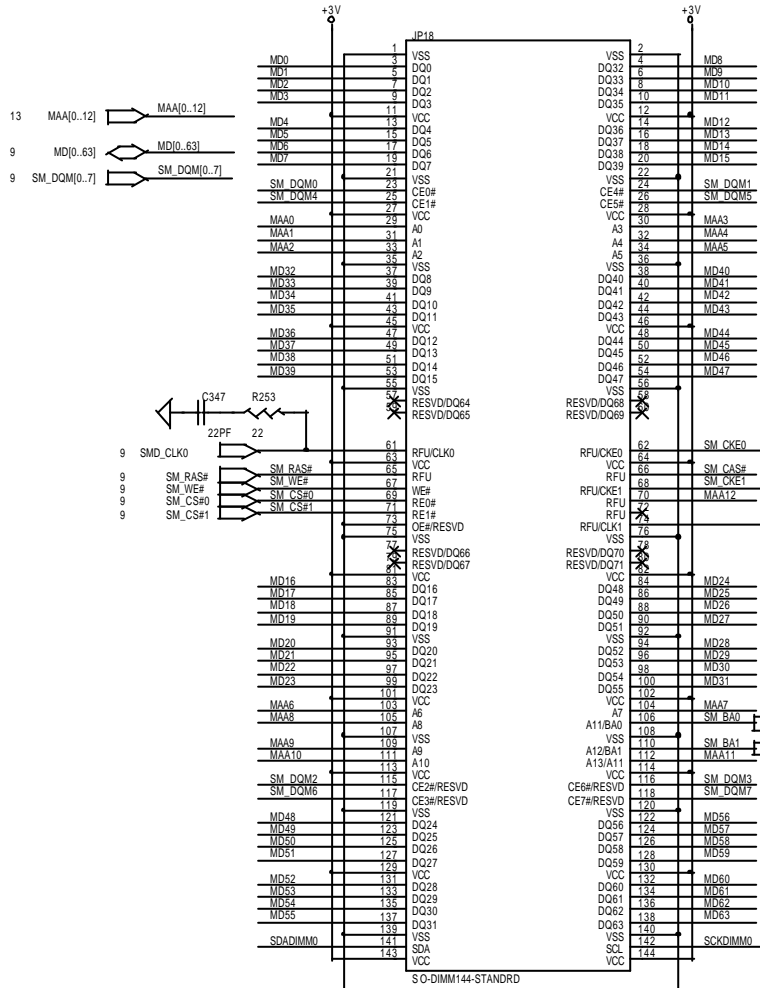
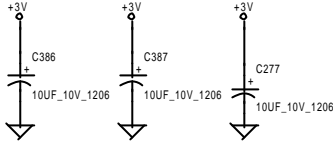
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**SO-DIM 144 PINS  
RAM MODULE CONN.**

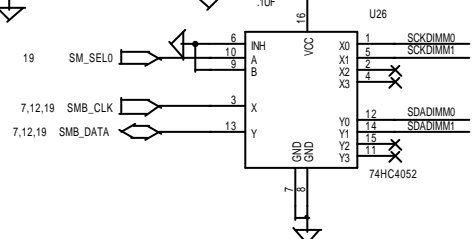
**BANK 0/1**

**BANK 2/3**

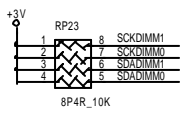


DIMM0

DIMM1



SM_SEL0	XY
0	SCKDIMM0
1	SCKDIMM1



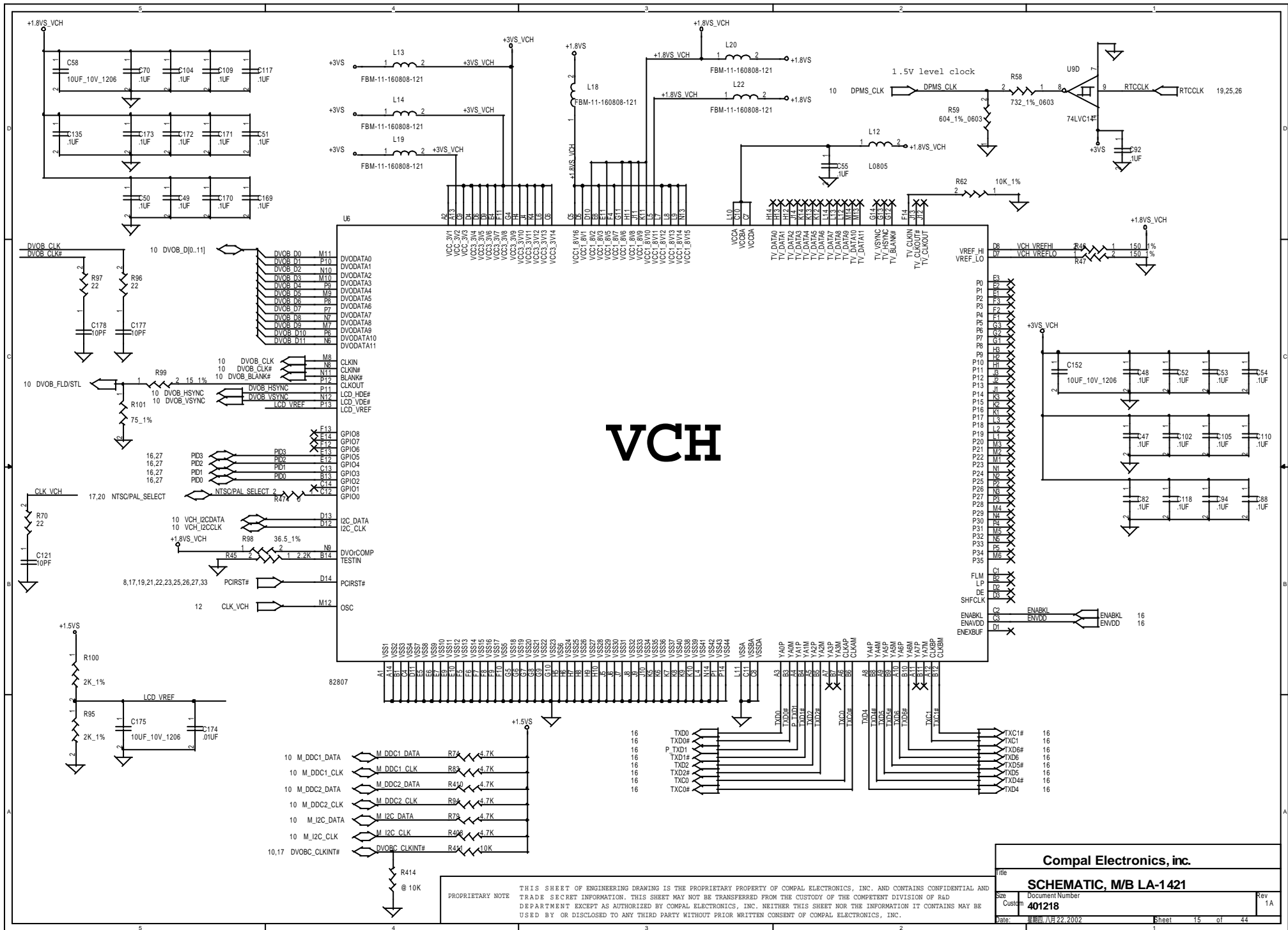
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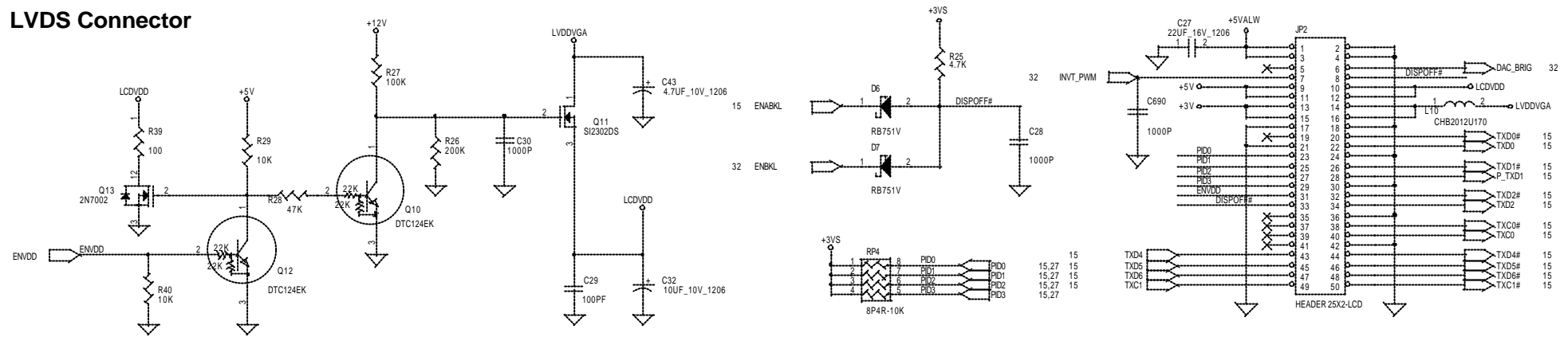


# VCH

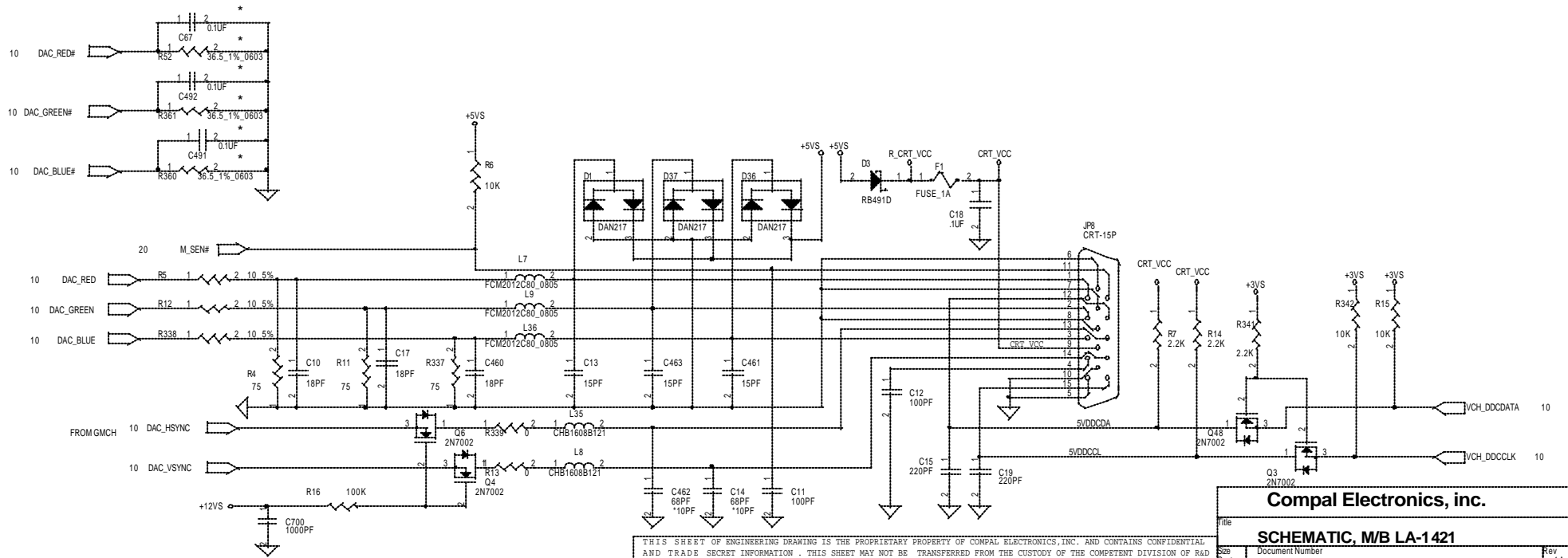
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# LVDS Connector



# CRT Connector



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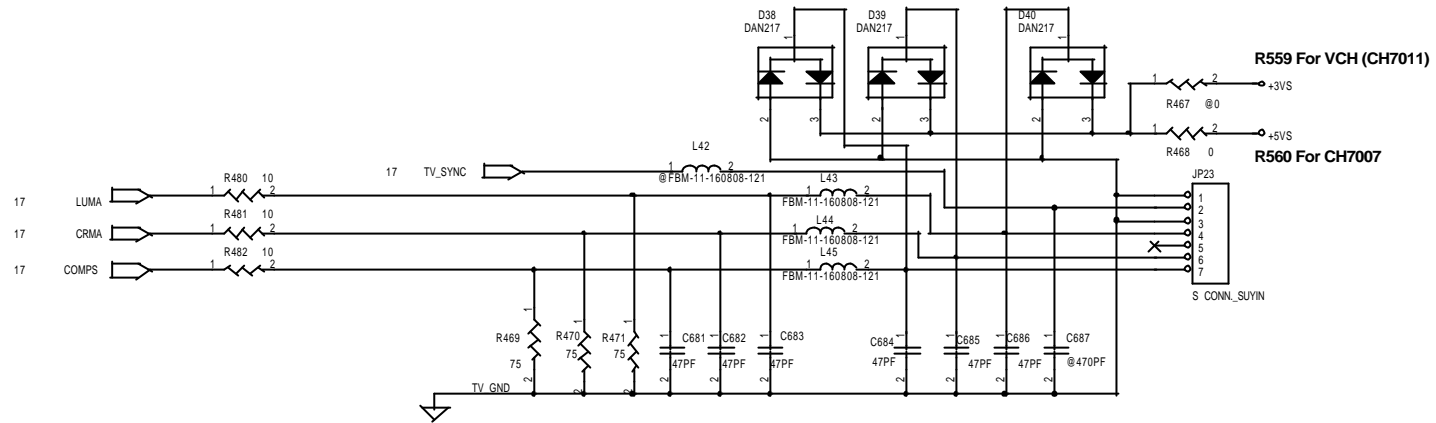
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# TV\_OUT CONN.



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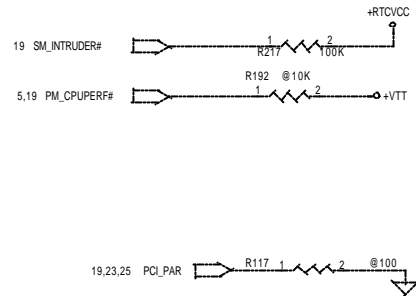
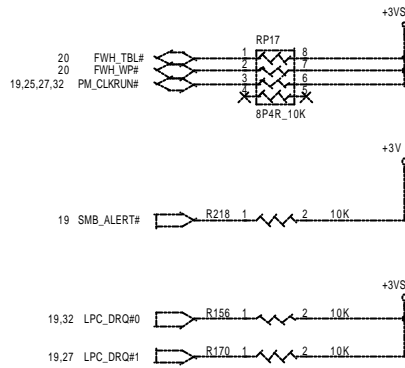
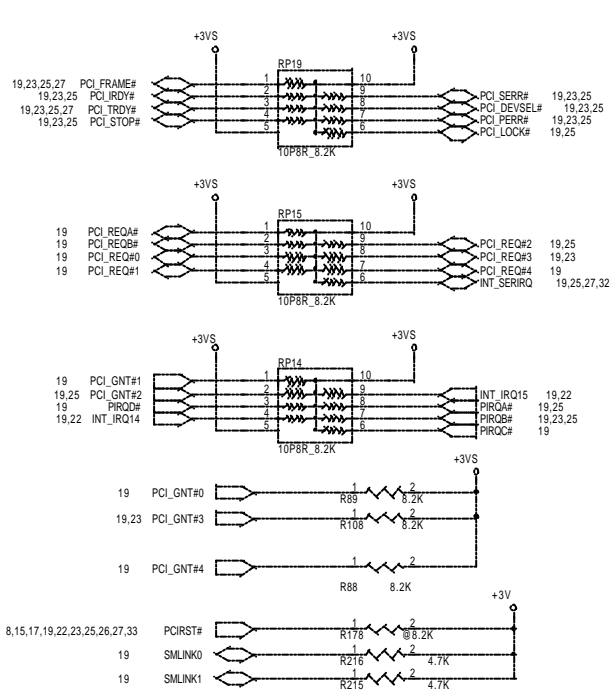
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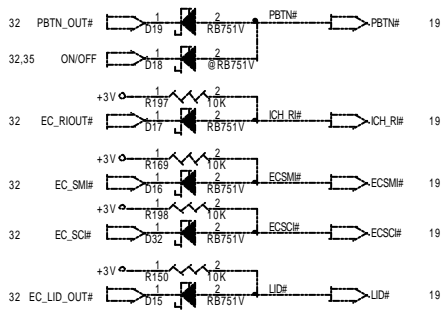




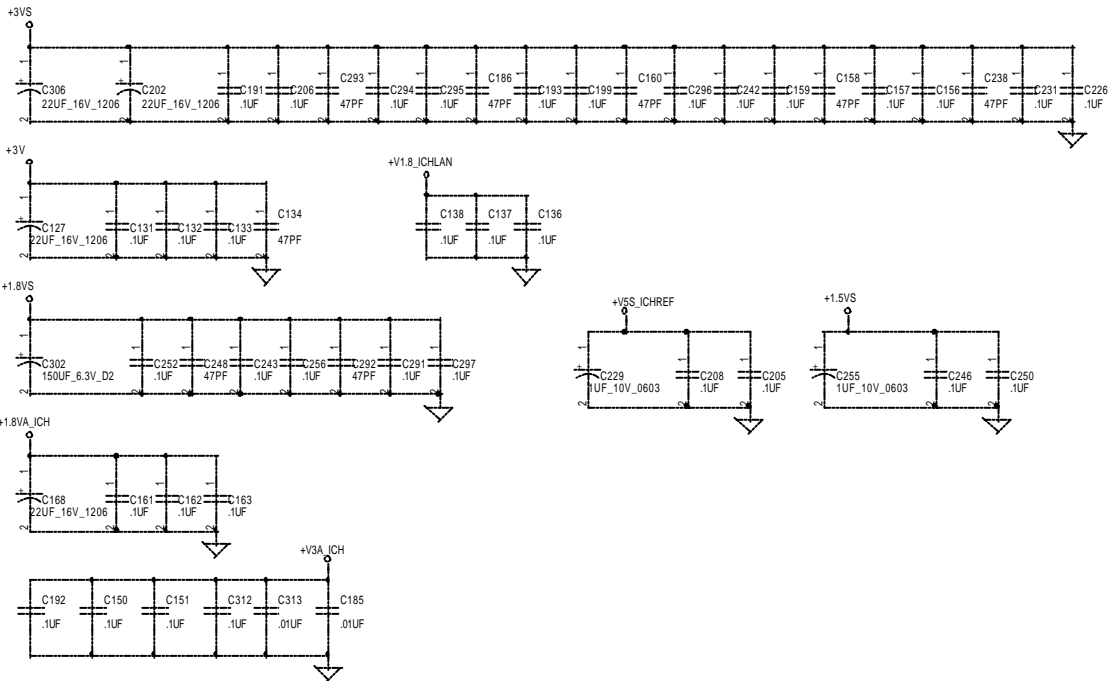
# ICH3-M PullUp Resistor



# Break Event Between ICH3-M and EC591



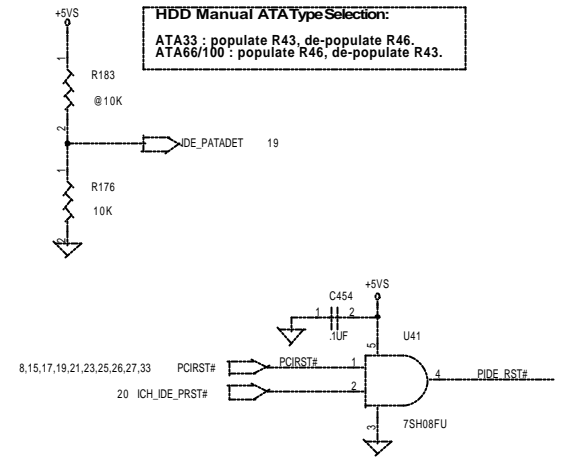
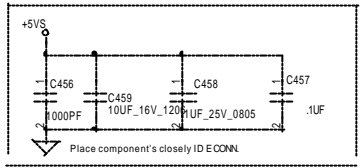
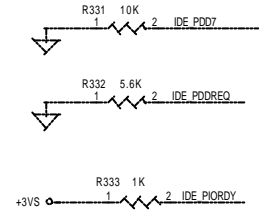
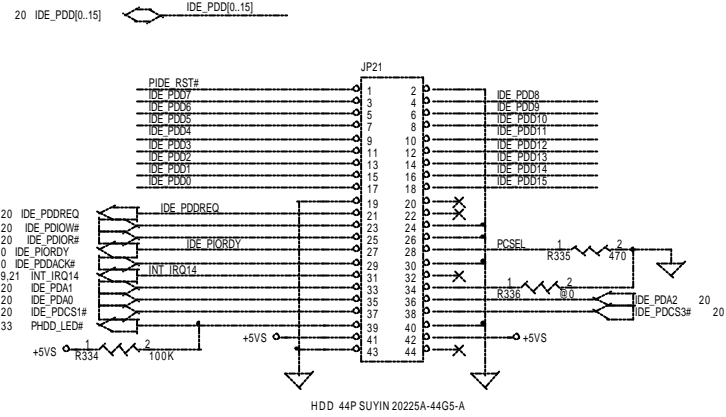
# ICH3-M Decoupling Capacitor



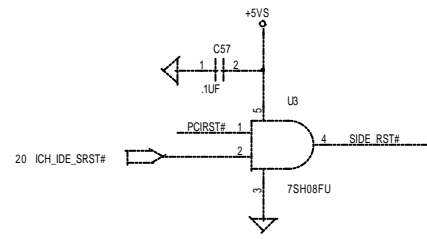
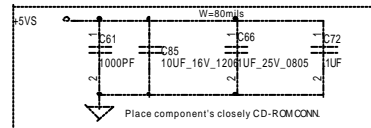
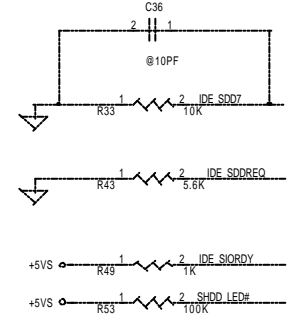
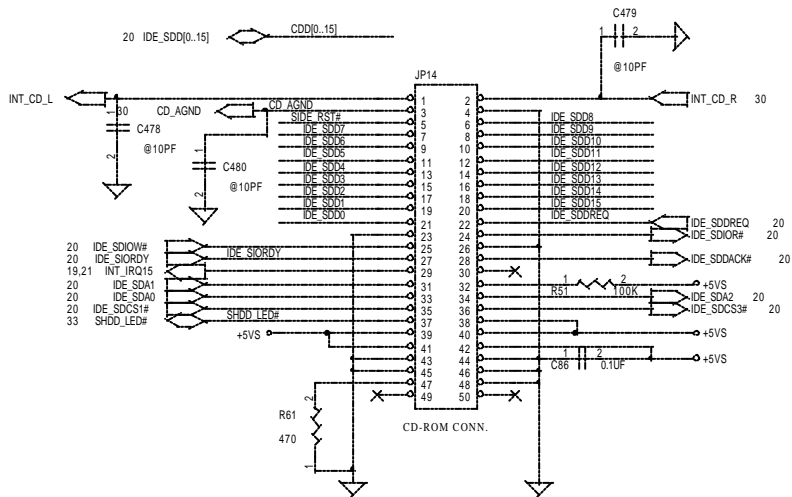
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# IDE Module CONN.

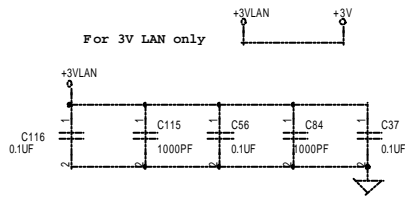
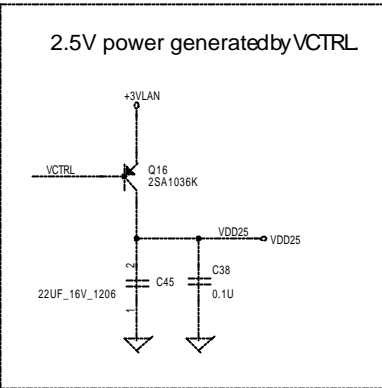
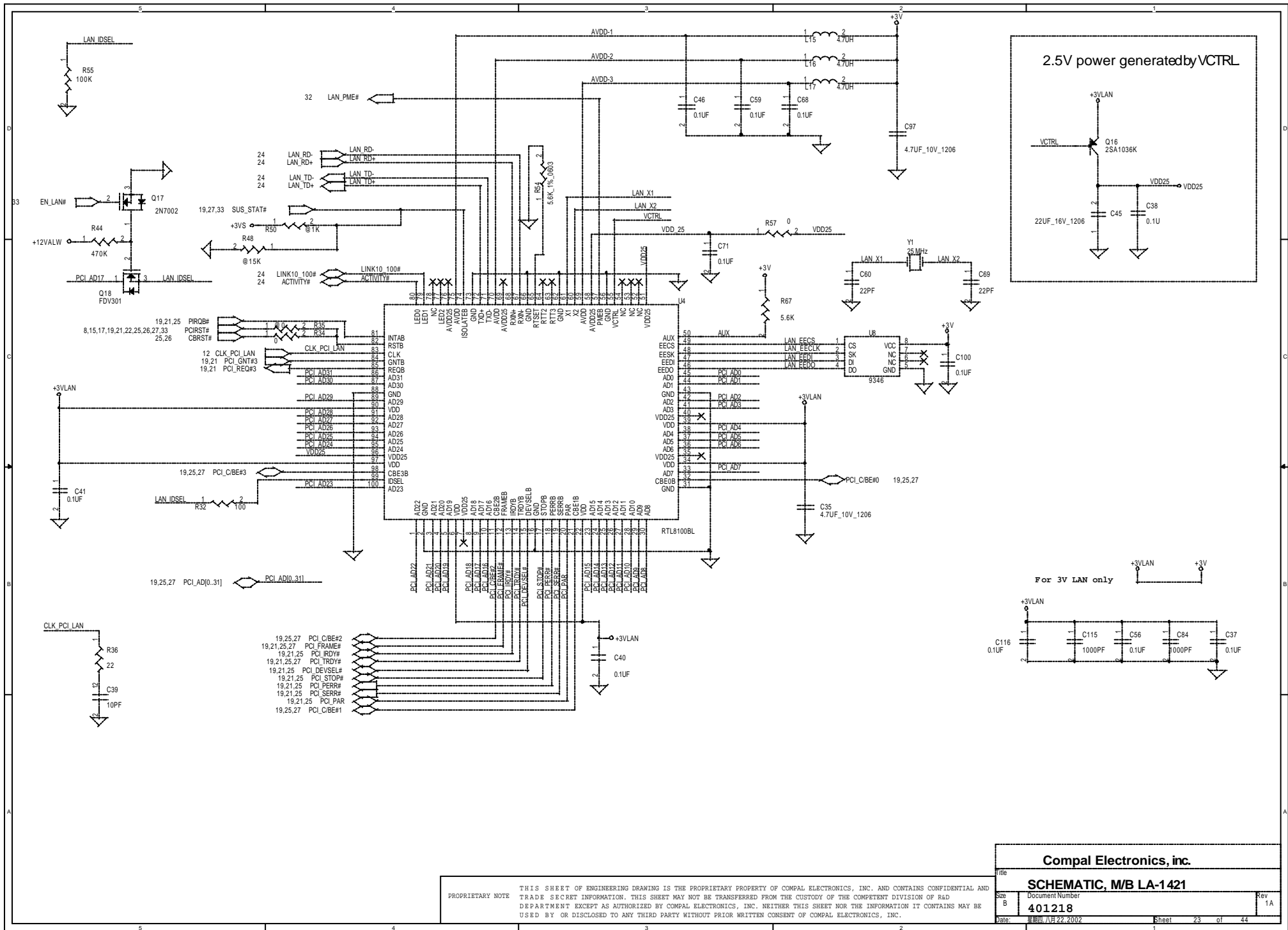


# CD-ROM Module CONN.



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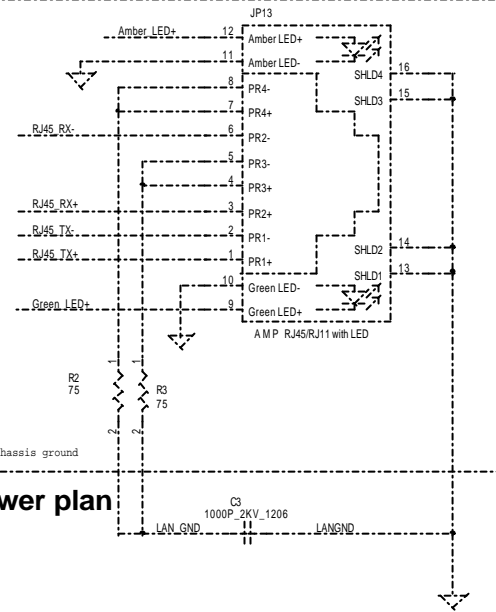
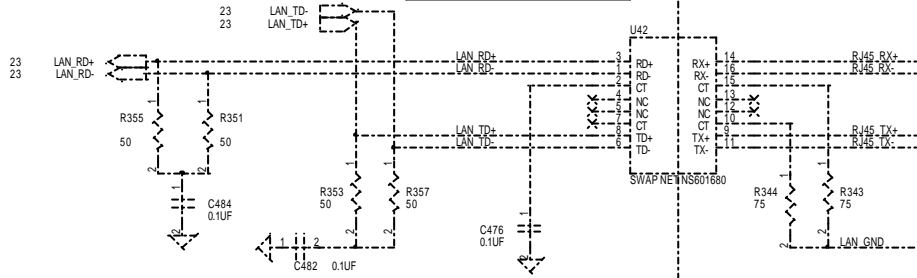
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LAN Transformer and Conn.

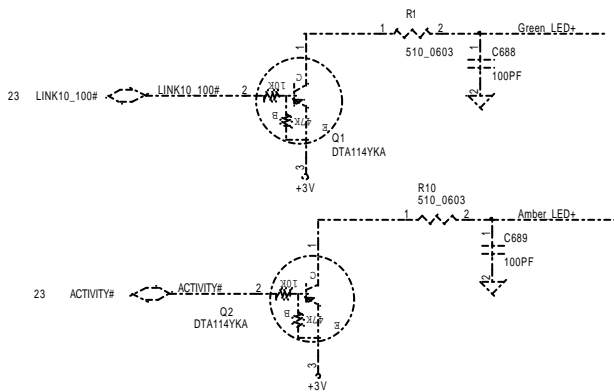
Keep Out 40mil

Layout Note  
H0013 pls close to  
conn.



Termination plane should be copied to chassis ground

LAYOUT NOTICE: This area do not connect to power plan  
include Vcc and GND in any layer



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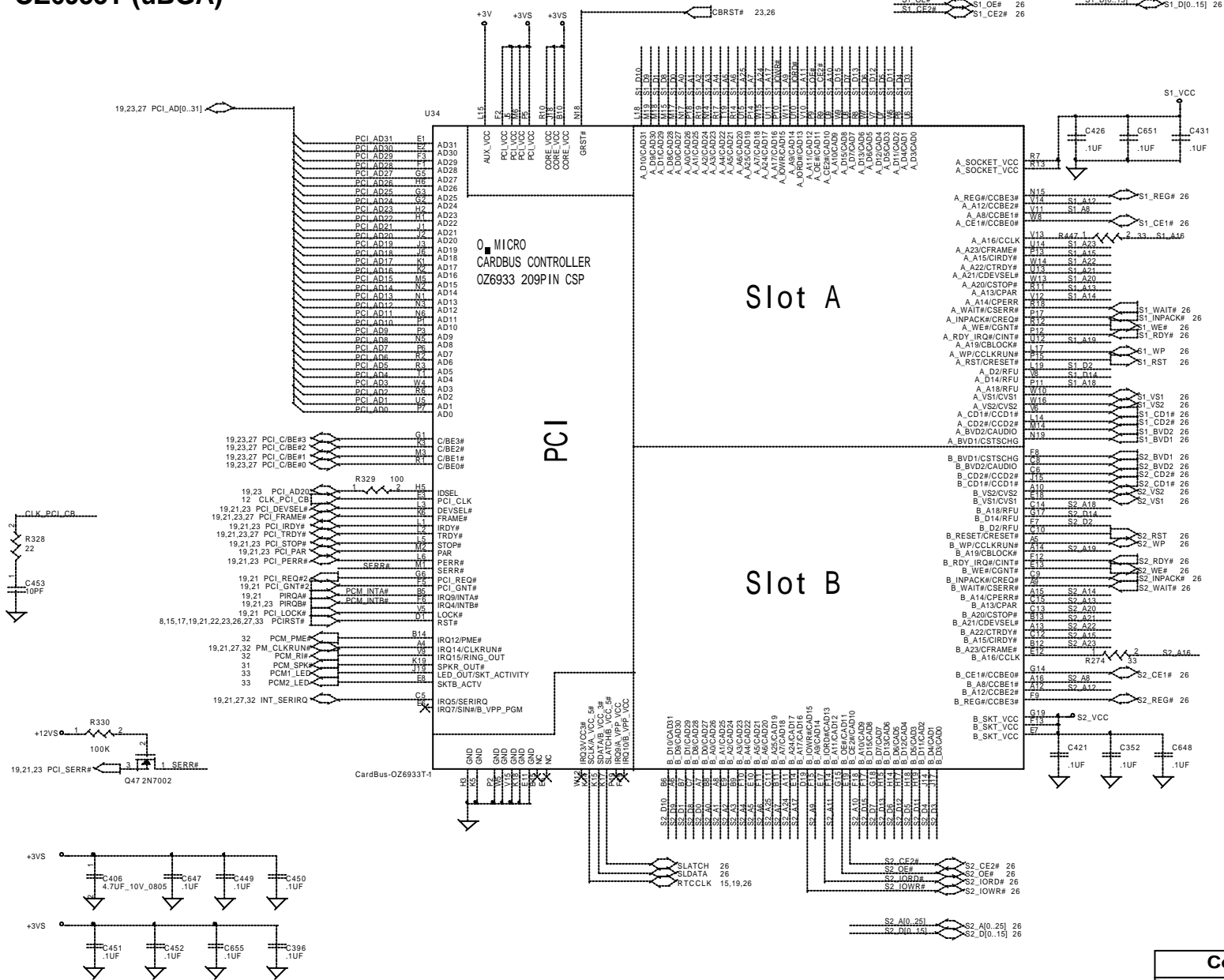
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# CardBus Controller OZ6933T (uBGA)



Micro  
CARDBUS CONTROLLER  
OZ6933 209PIN CSP

Slot A

Slot B

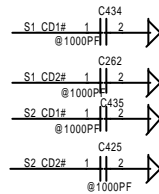
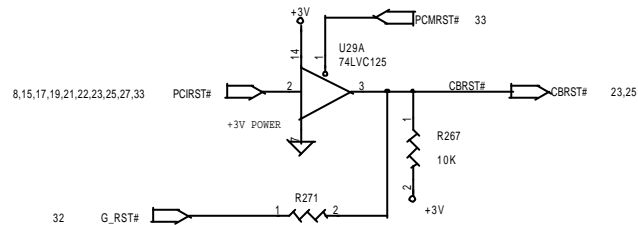
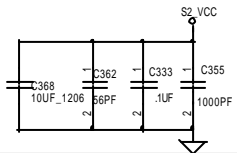
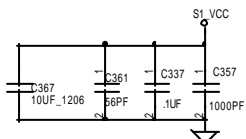
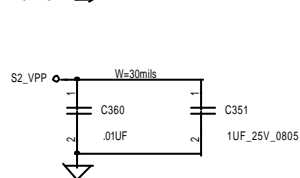
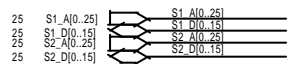
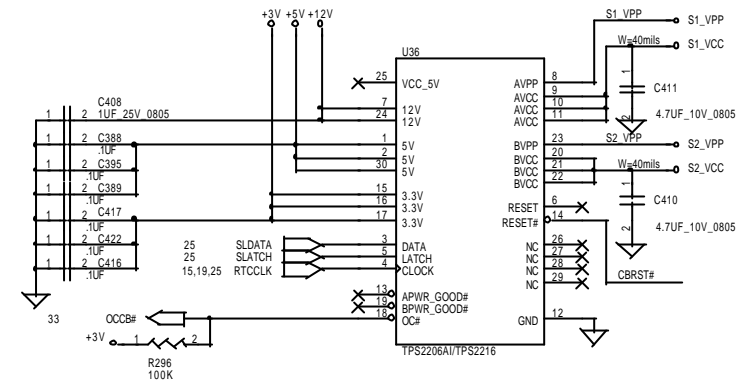
PCI

CardBus-OZ6933T-1

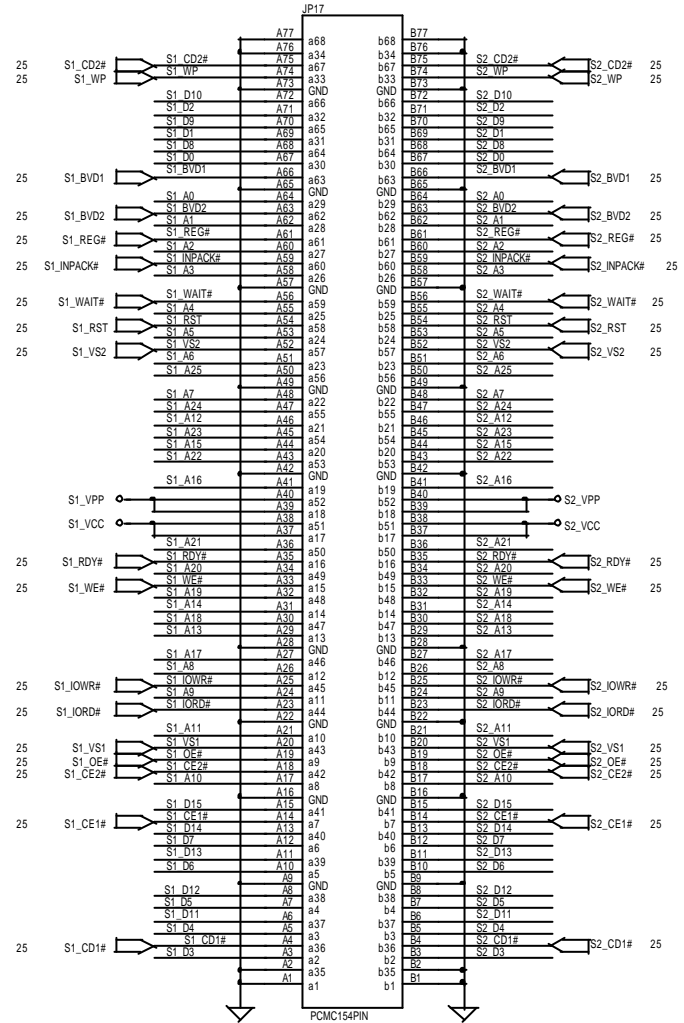
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# PCMCIA POWER CTRL.



# CARDBUS SOCKET

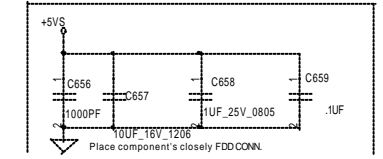
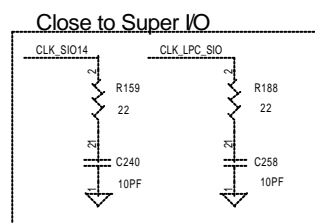
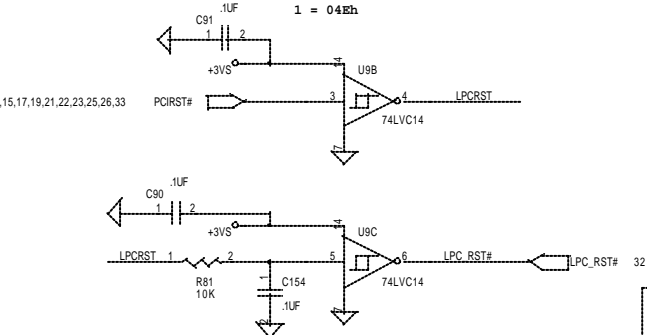
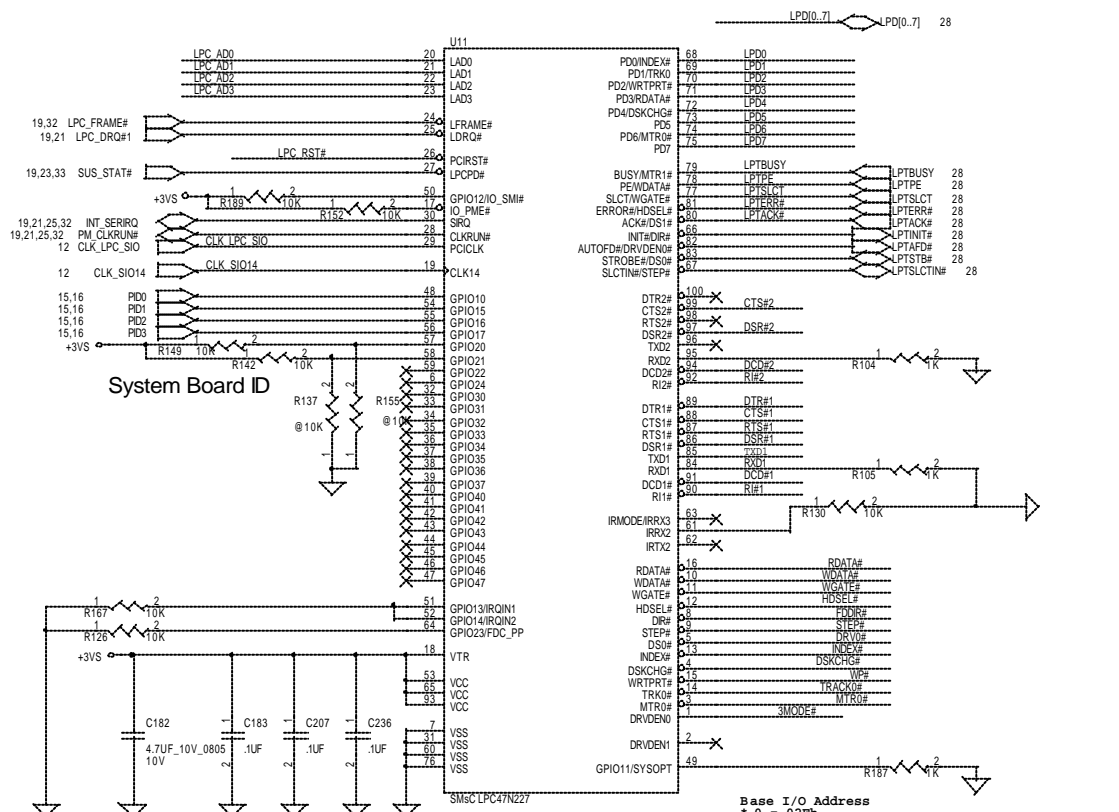


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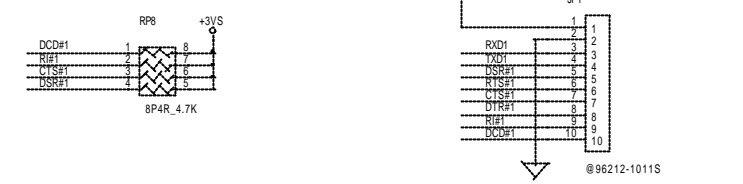
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rfile		
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# SUPER I/O SMC FDC47N227

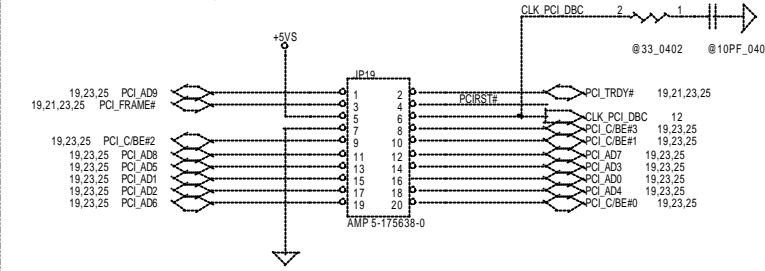
19.32 LPC\_AD[0..3]  $\leftrightarrow$  LPC\_ADIO\_3[ ]



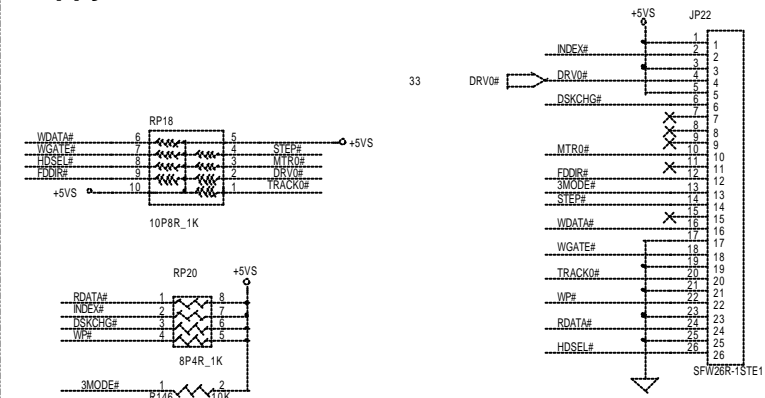
## ACPI Debug Connector



## Port 80 Debug Card Connector



## Floppy Connector



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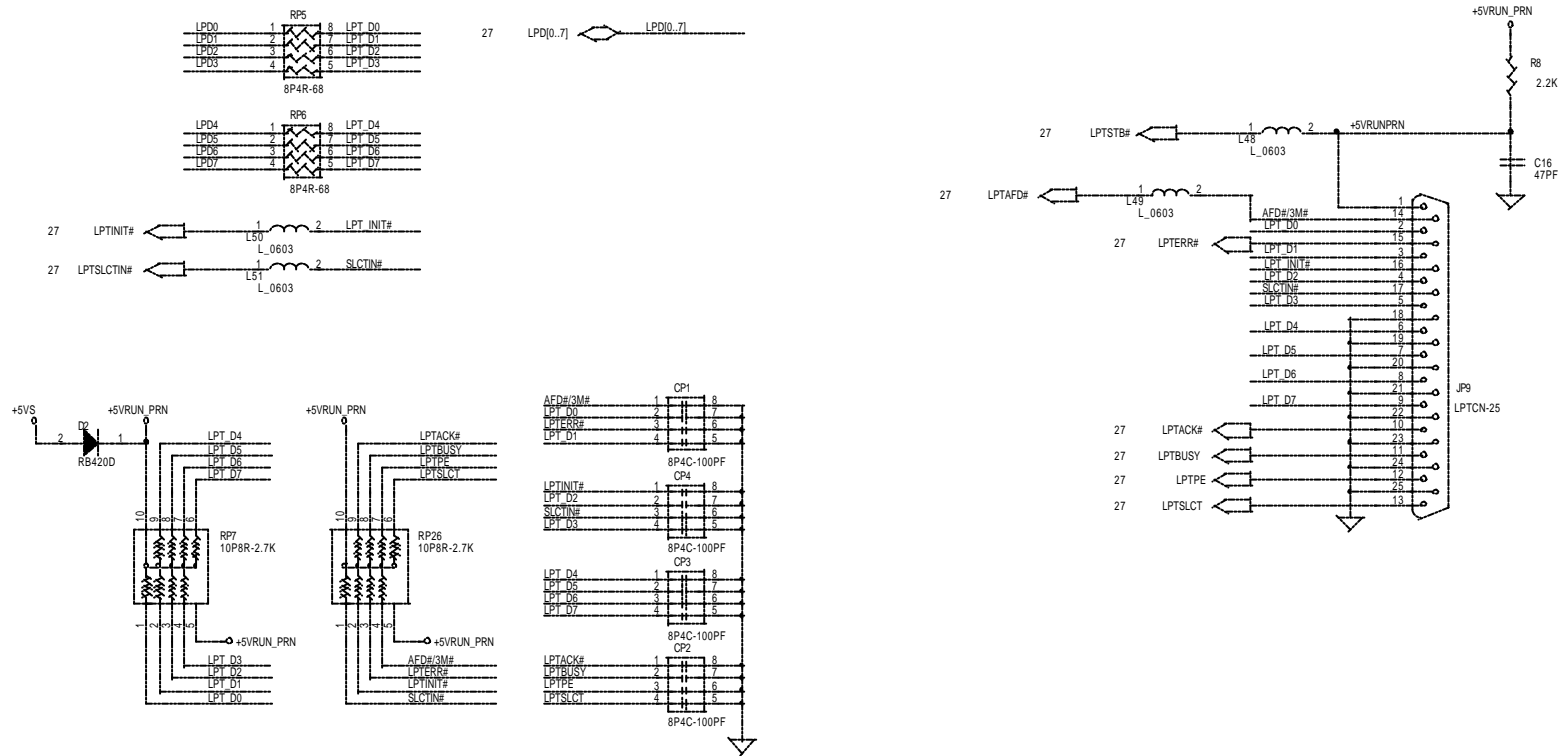
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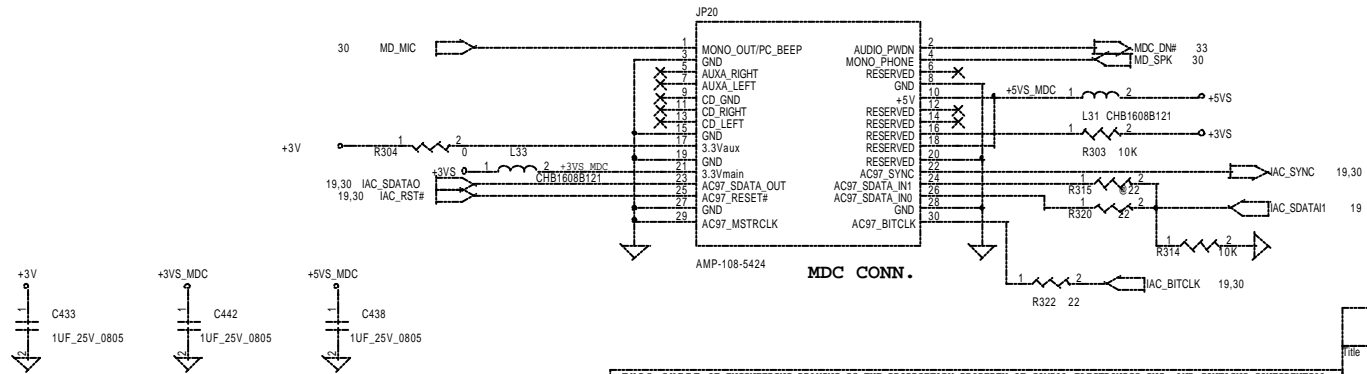
Date: 2002/11/22

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# Parallel Port



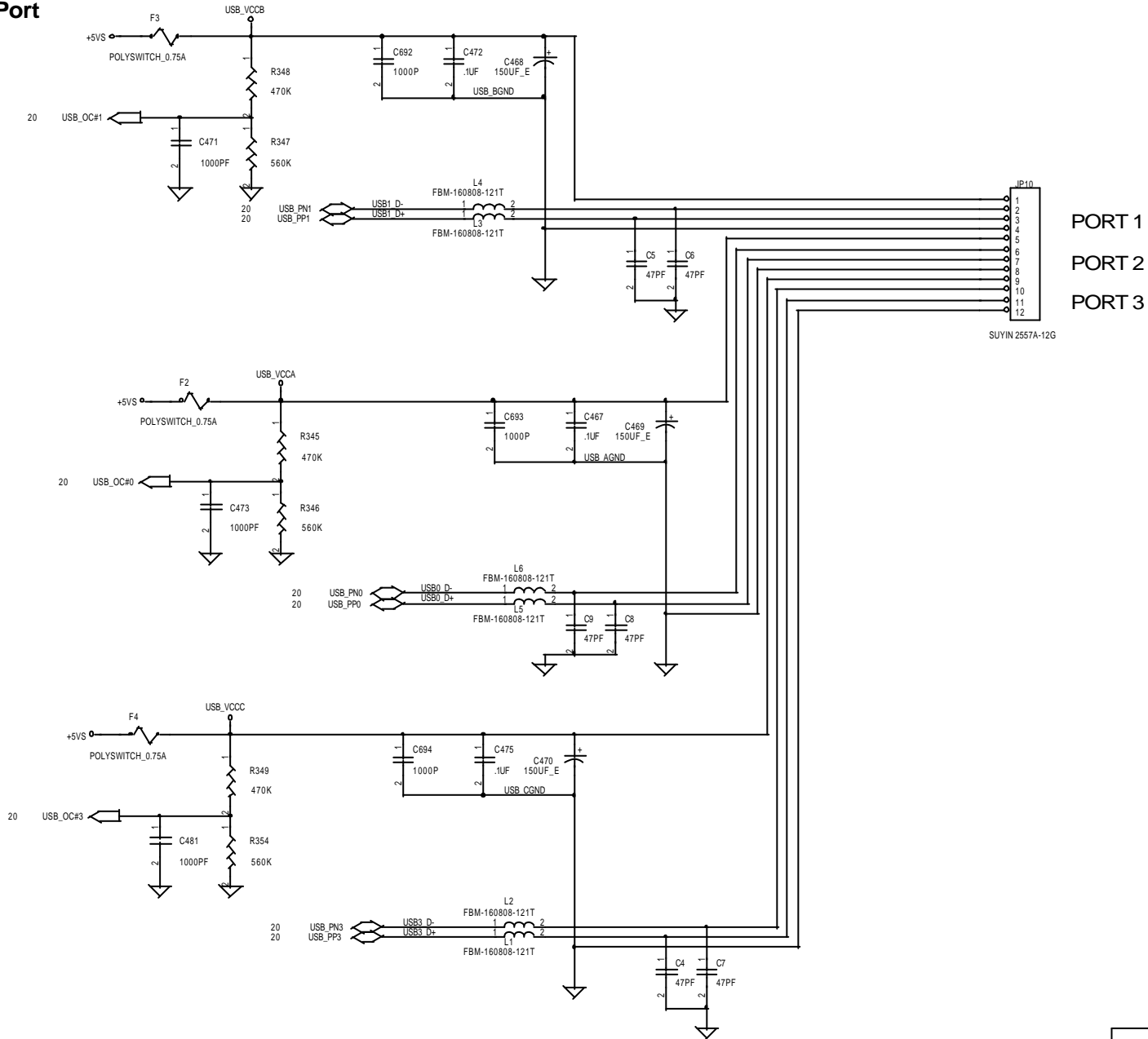
# MDC Connector



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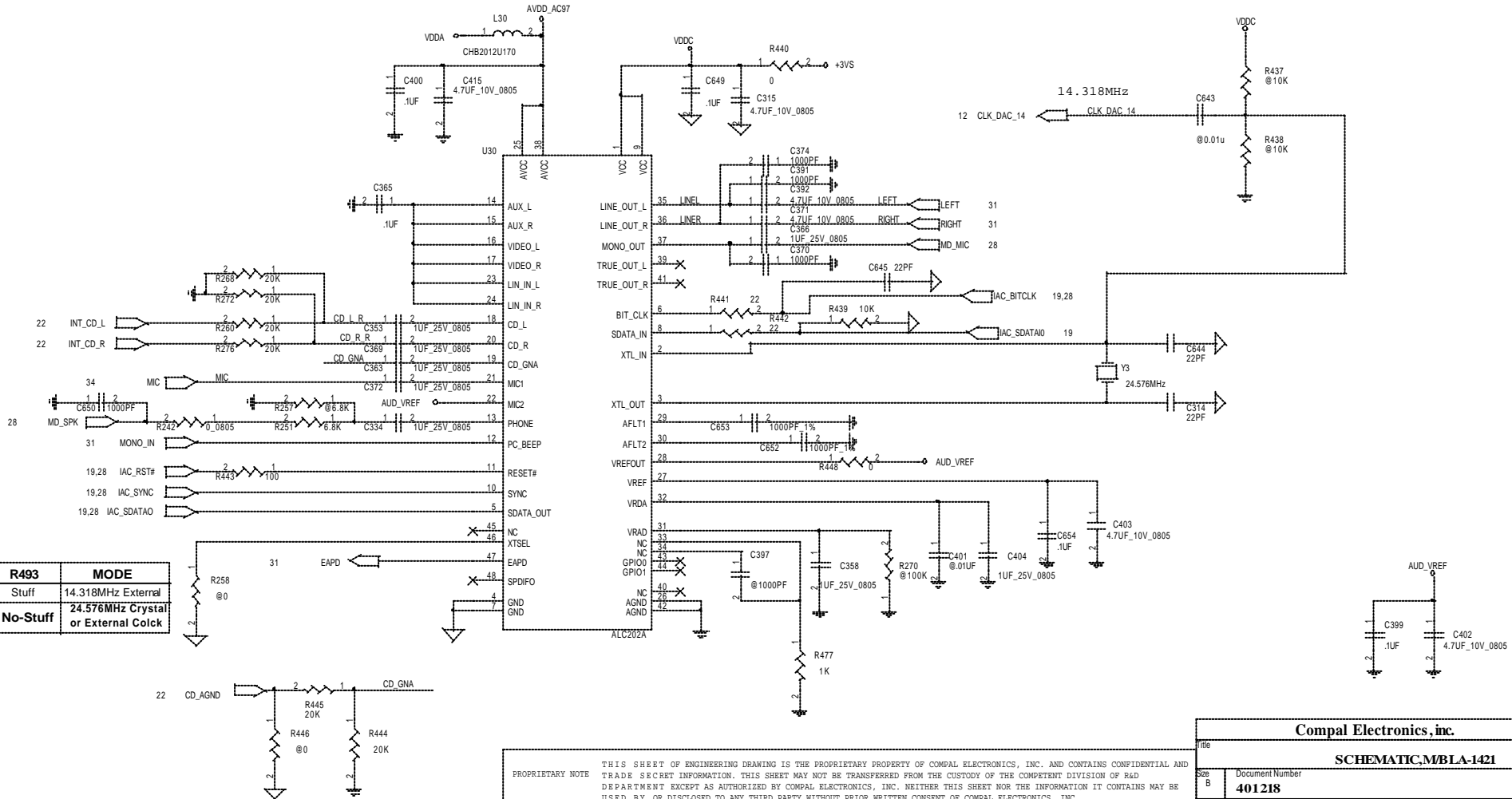
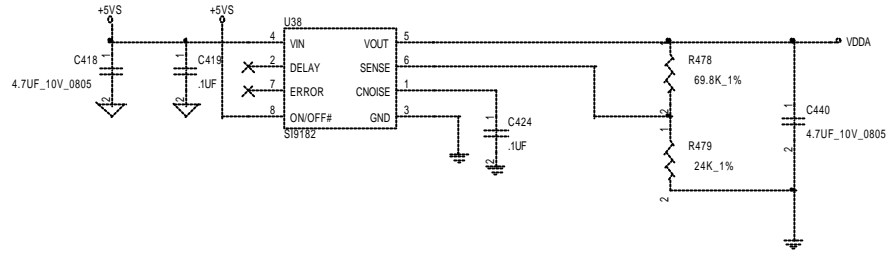
# USB Port



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# AC97 Audio Codec



R493	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

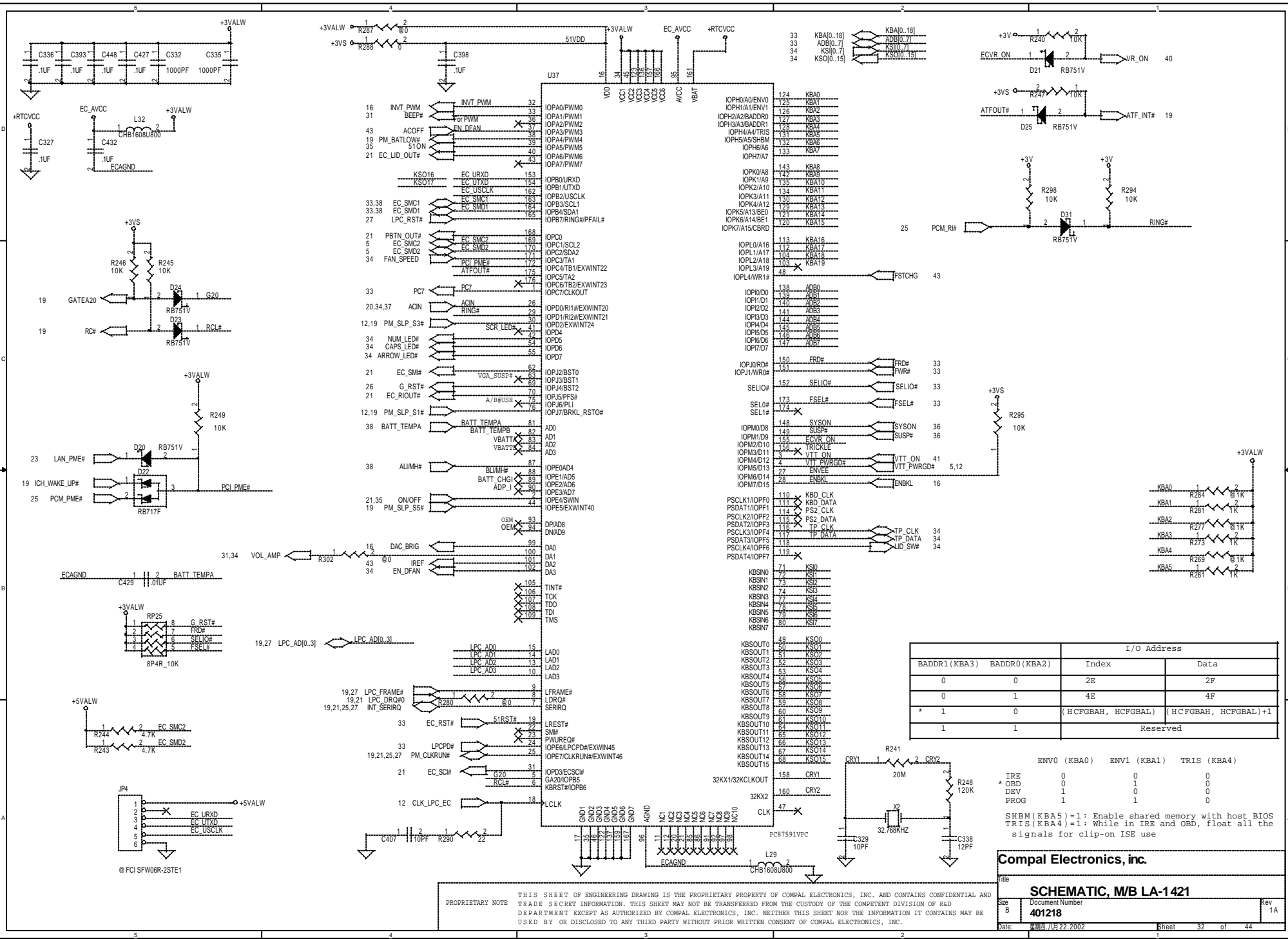
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16	INVT_PWM	32	IOPA0/PWM0
31	BEEP#	33	IOPA1/PWM1
	OP_PWM	36	IOPA2/PWM2
43	ACOFF	37	IOPA3/PWM3
	EN_DFAN	38	IOPA4/PWM4
19	PM_BATLOW#	39	IOPA5/PWM5
35	S1YON	40	IOPA6/PWM6
21	EC_LID_OUT#	43	IOPA7/PWM7
	KSO16	153	IOPB0/URXD
	EC_URXD	154	IOPB1/UTXD
	EC_UTXD	162	IOPB2/USCLK
	EC_USCLK	163	IOPB3/SMD1
33,38	EC_SMC1	164	IOPB4/SDA1
33,38	EC_SMD1	165	IOPB7/RING#/PFAIL#
27	LPC_RST#	168	IOPC0
		169	IOPC1/SCL2
21	PBTN_OUT#	170	IOPC2/SDA2
5	EC_SMC2	171	IOPC3/TA1
5	EC_SMD2	172	IOPC4/TB1/EXWINT22
34	FAN_SPEED	173	IOPC5/TA2
		175	IOPC6/TB2/EXWINT23
		176	IOPC7/CLKOUT
33	PC7	26	IOPD0/RH#/EXWINT20
20,34,37	ACIN	29	IOPD1/RH#/EXWINT21
		30	IOPD2/EXWINT24
12,19	PM_SLP_S3#	31	IOPD3
		32	IOPD4
34	NUM_LED#	33	IOPD5
34	CAPS_LED#	34	IOPD6
34	ARROW_LED#	35	IOPD7
		62	IOPJ0/RD#
21	EC_SM#	63	IOPJ1/WR0#
	VGA_SUSP#	65	SEL0#
26	G_RST#	69	SEL0#
21	EC_RIOUT#	70	SEL0#
	A/BHUBSE	76	SEL1#
12,19	PM_SLP_S1#	77	SEL1#
		81	IOPM0/D8
38	BATT_TEMP#	82	IOPM1/D9
	BATT_TEMP#	83	IOPM2/D10
	VBATT#	84	IOPM3/D11
	VBATT#	84	IOPM4/D12
		87	IOPM5/D13
38	ALIMH#	88	IOPM6/D14
	BLIM#	89	IOPM7/D15
	BATT_CHG#	90	PSCLK1/OPF0
	ADP_1	90	PSDAT1/OPF1
21,35	ON/OFF	92	PSCLK2/OPF2
19	PM_SLP_S5#	92	PSDAT2/OPF3
		93	PSCLK3/OPF4
		93	PSDAT3/OPF5
		94	PSCLK4/OPF6
		94	PSDAT4/OPF7
		99	KBSIN0
		100	KBSIN1
		101	KBSIN2
		102	KBSIN3
		103	KBSIN4
		104	KBSIN5
		105	KBSIN6
		106	KBSIN7
		107	KBSOUT0
		108	KBSOUT1
		109	KBSOUT2
		110	KBSOUT3
		111	KBSOUT4
		112	KBSOUT5
		113	KBSOUT6
		114	KBSOUT7
		115	KBSOUT8
		116	KBSOUT9
		117	KBSOUT10
		118	KBSOUT11
		119	KBSOUT12
		120	KBSOUT13
		121	KBSOUT14
		122	KBSOUT15
		158	CRV1
		160	CRV2
		160	CRV2
		47	CLK
		47	CLK

I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

	ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM (KBA5)=1: Enable shared memory with host BIOS  
 TRIS (KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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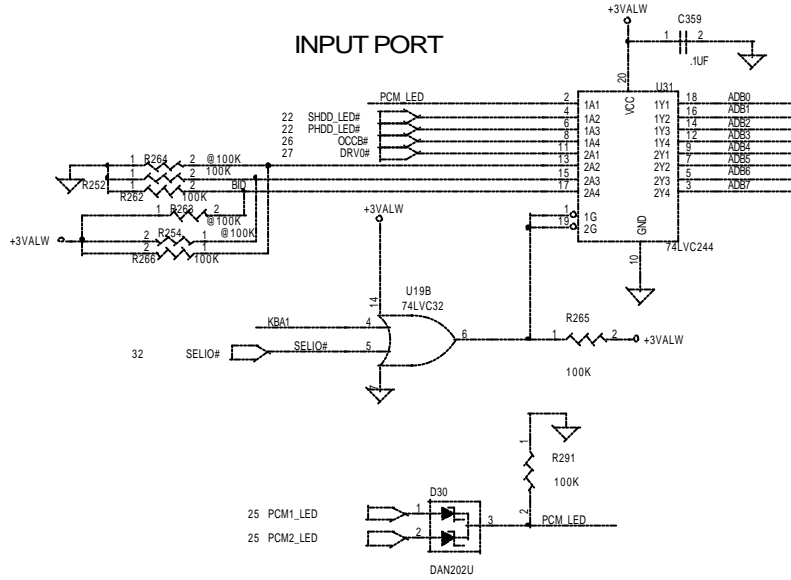
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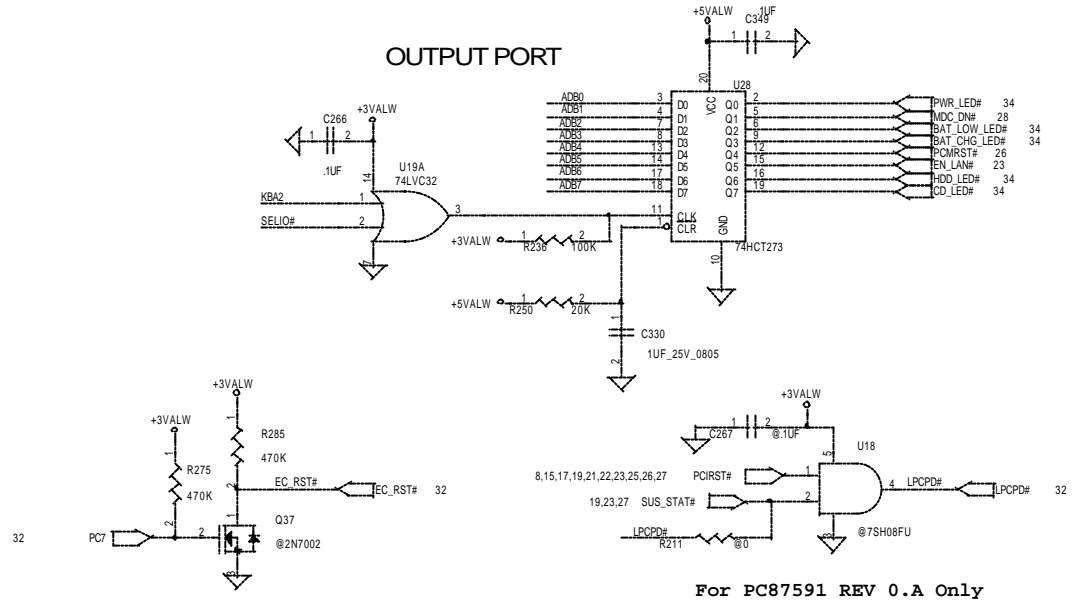


# EXT I/O PORT

## INPUT PORT

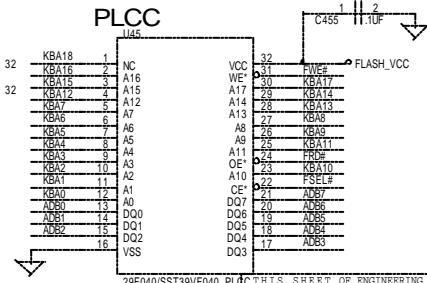
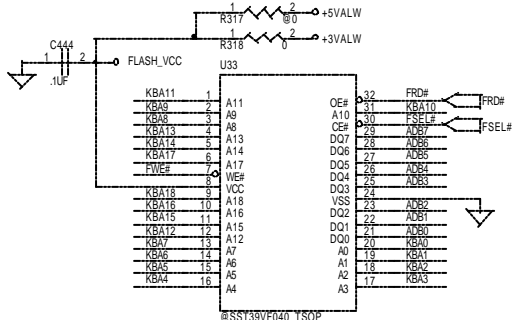
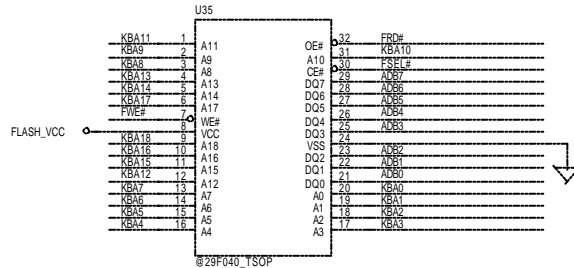
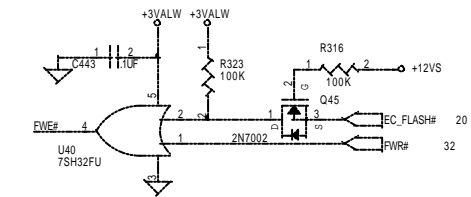


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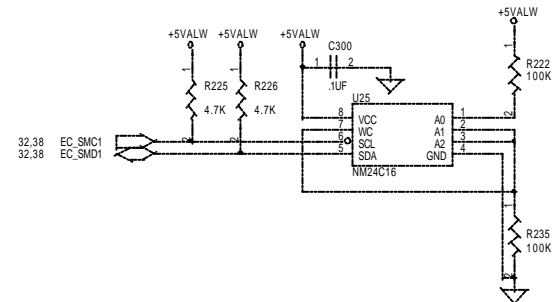


For PC87591 REV 0.A Only

# SYSTEM BIOS



# SMBus EEPROM



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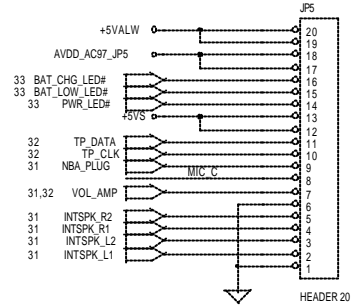
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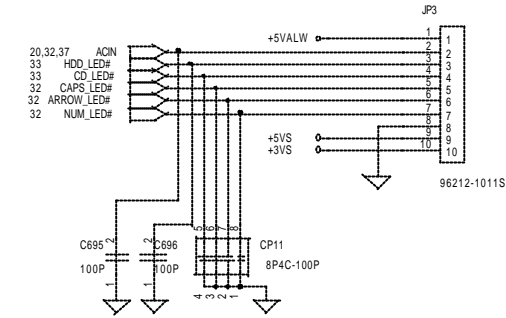
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# System Connector

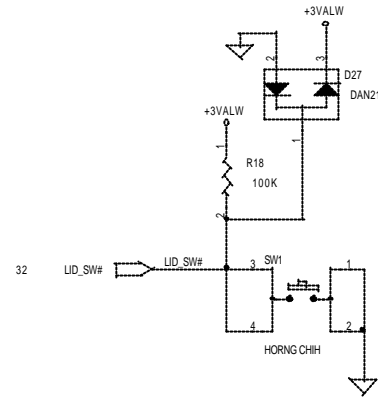
## Switch Board Connector



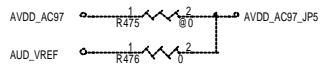
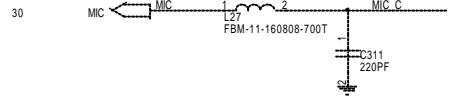
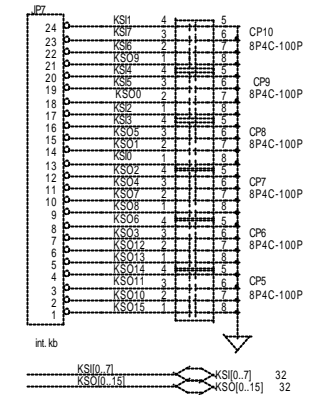
## LED Board Connector



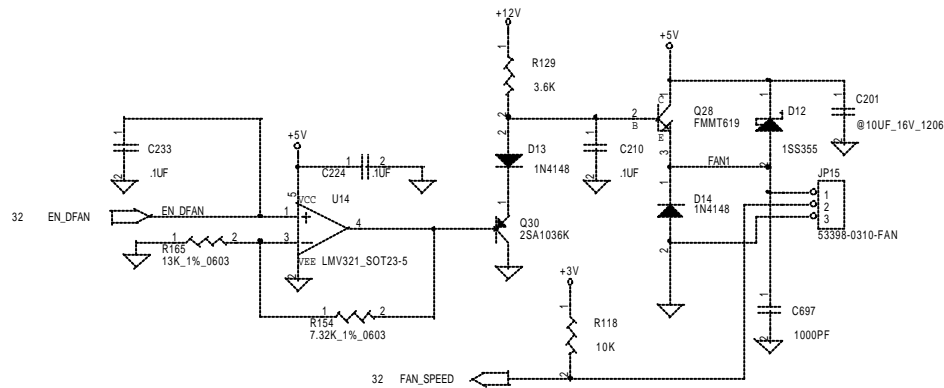
## LID Switch



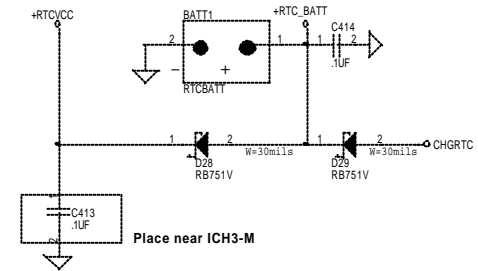
## Int. Keyboard Connector



## FAN Connector



## RTC Batt. Connector



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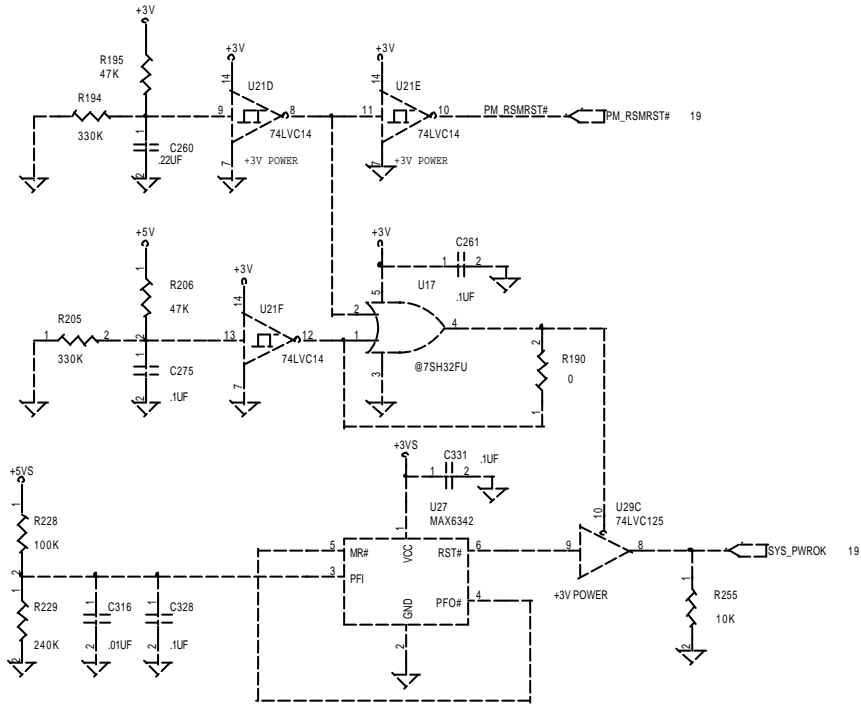
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File: SCHEMATIC, M/B LA-1421

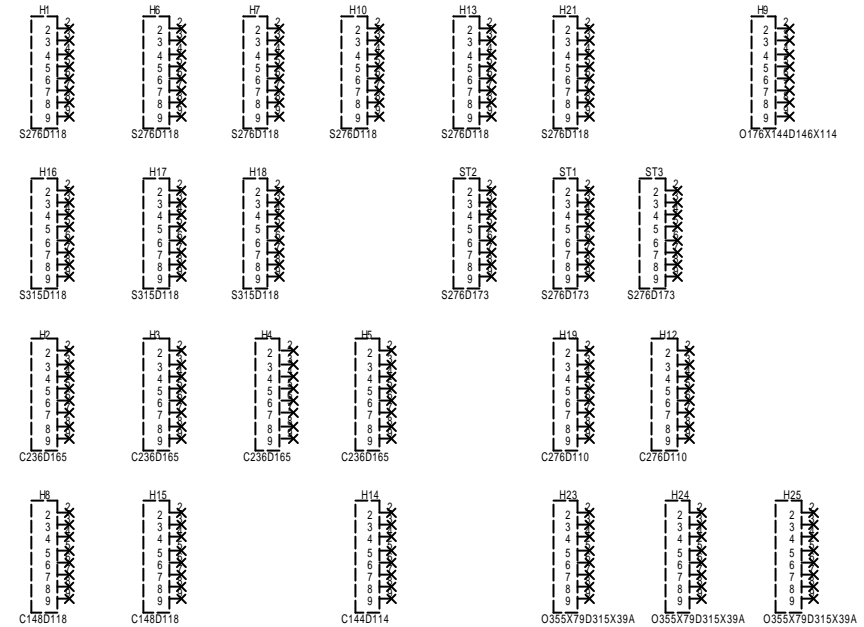
Size: B Document Number: 401218 Rev: 1A

Date: 2002/08/22 Sheet: 34 of 44

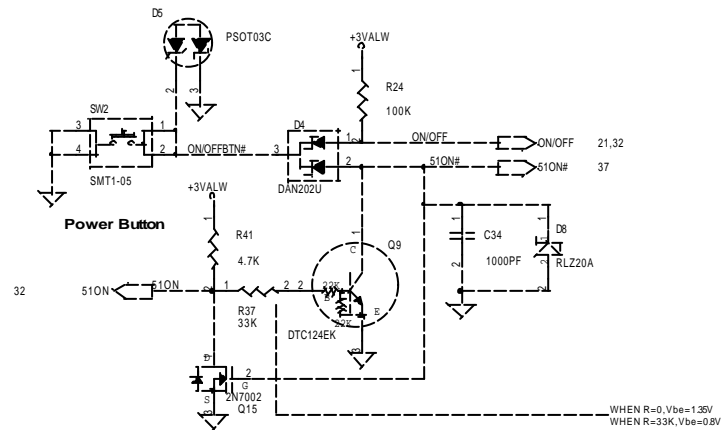
### South Bridge Power Good Circuit



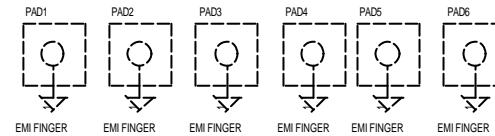
### Screw Hole



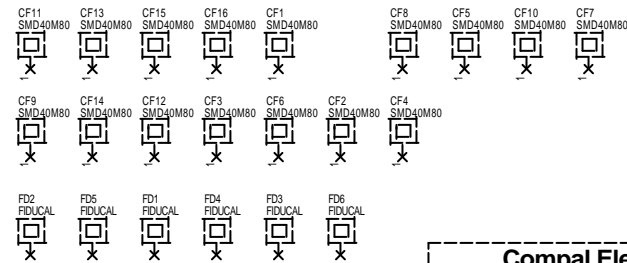
### Switch for Power Button



### EMI Finger



### Fiducial Mark



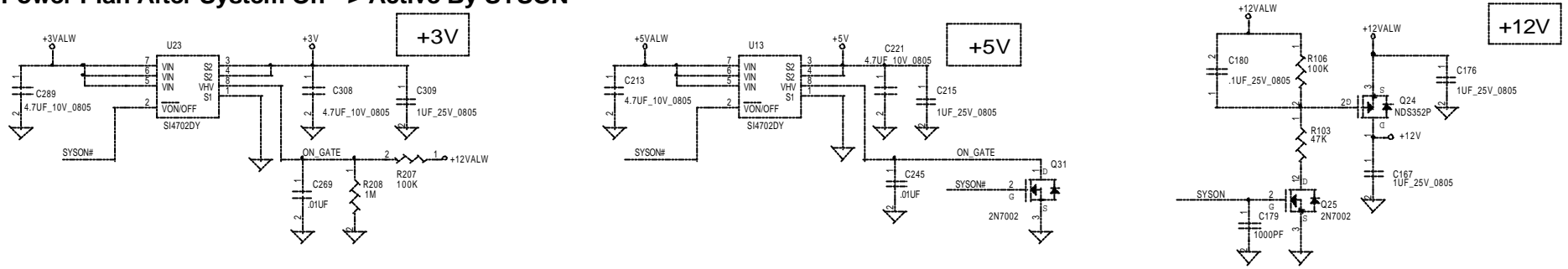
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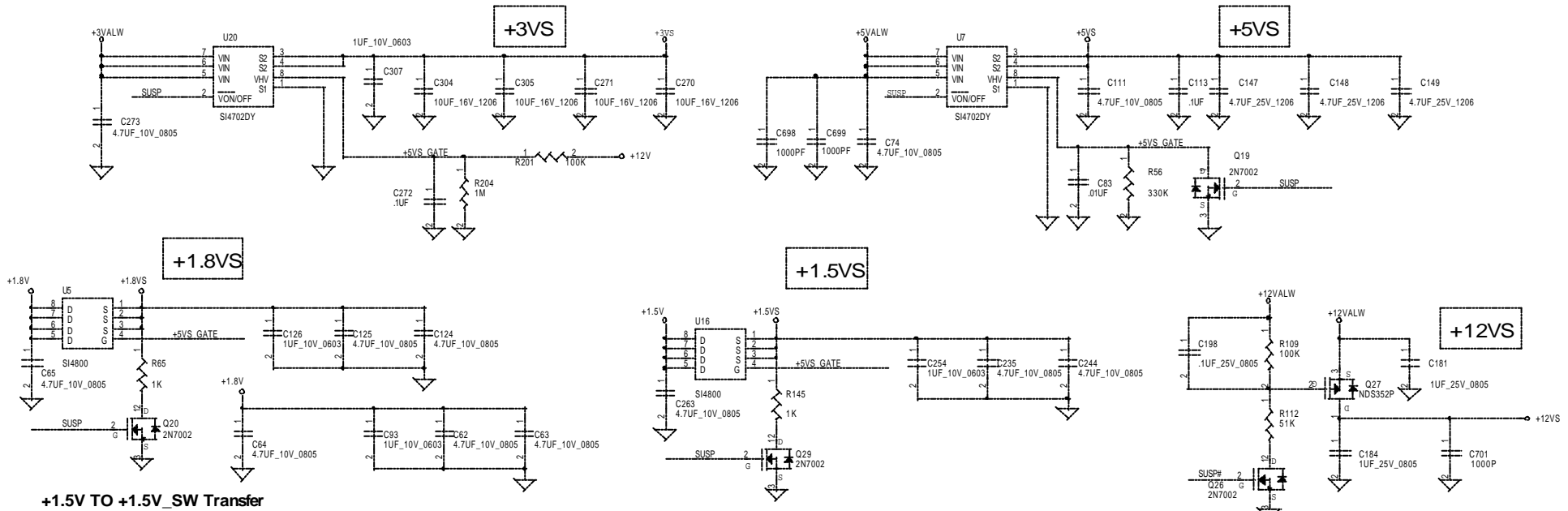
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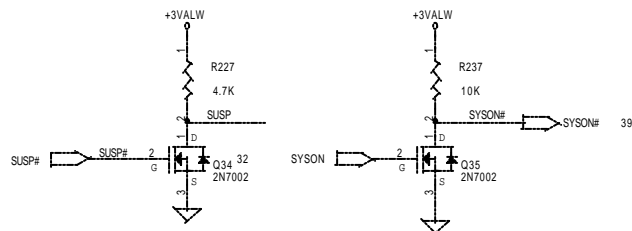
### Power Plan After System On --> Active By SYSON



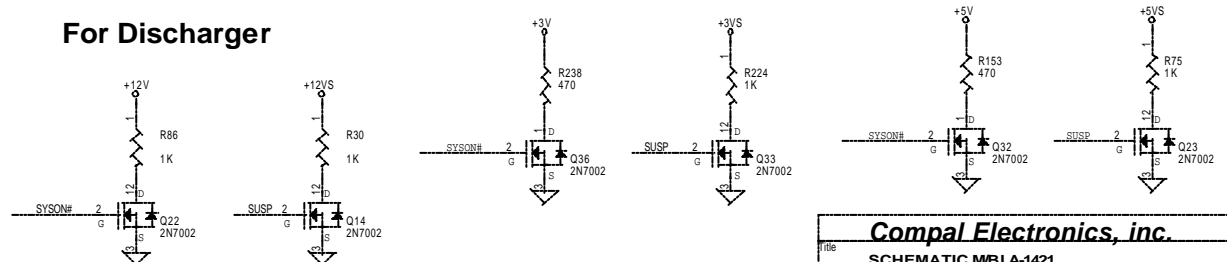
### Power Off During System Suspend(S3) --> Active By SUSP



### Signal Inverter



### For Discharger



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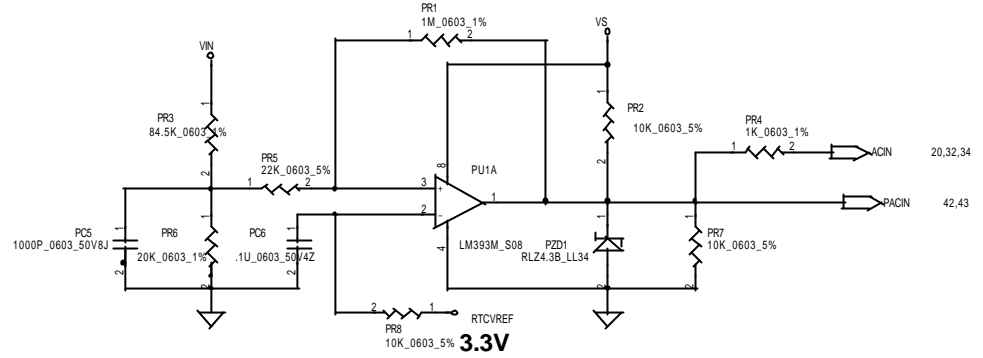
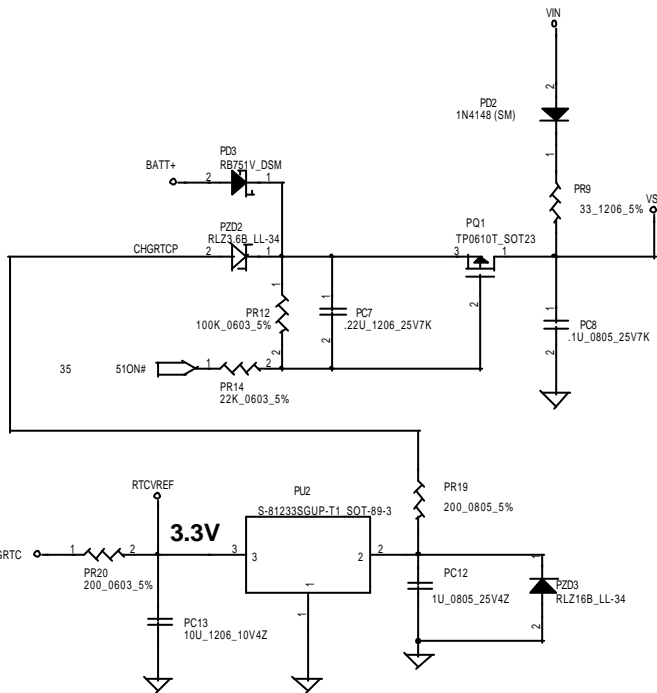
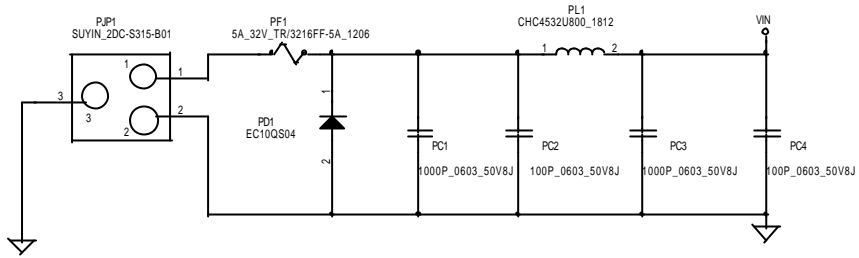
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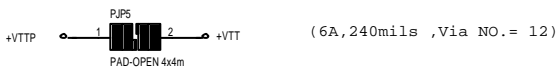
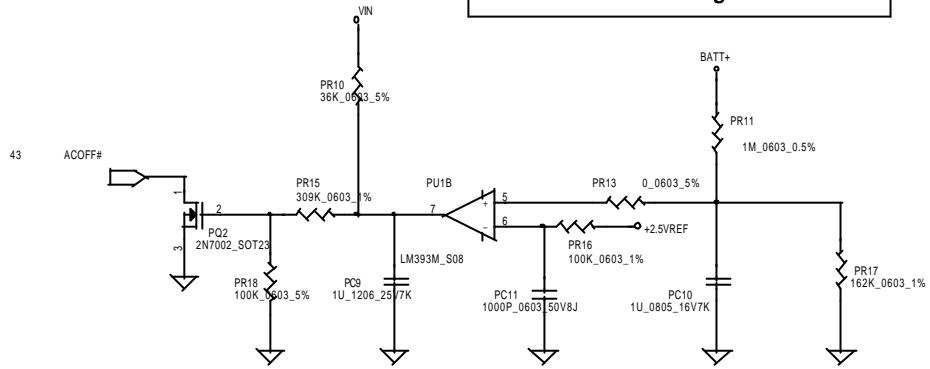
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### Vin Detector

High 18.764 17.901 17.063  
Low 17.745 16.903 16.038

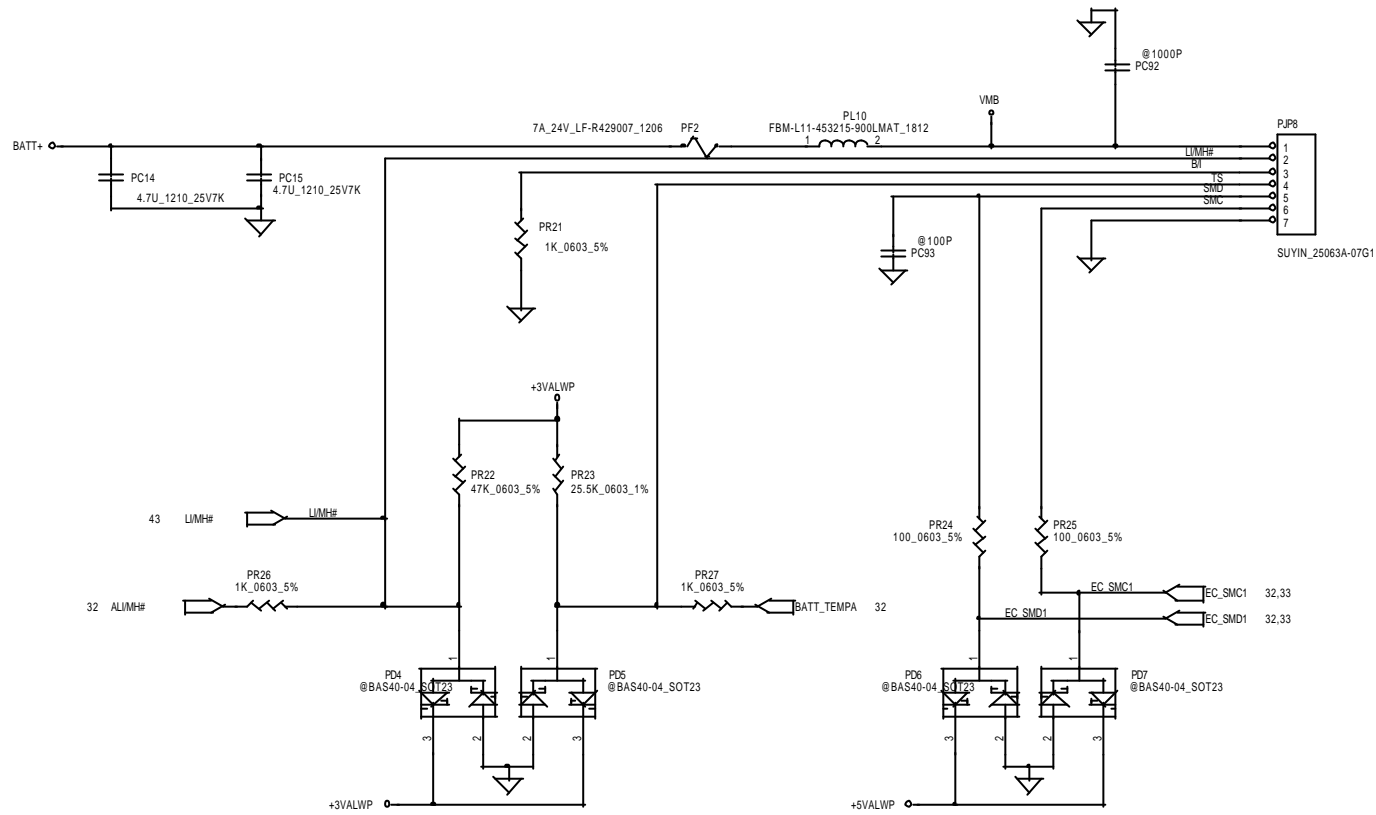


### 8 Cells LI-ION BAT Charger OVP : 18.059V



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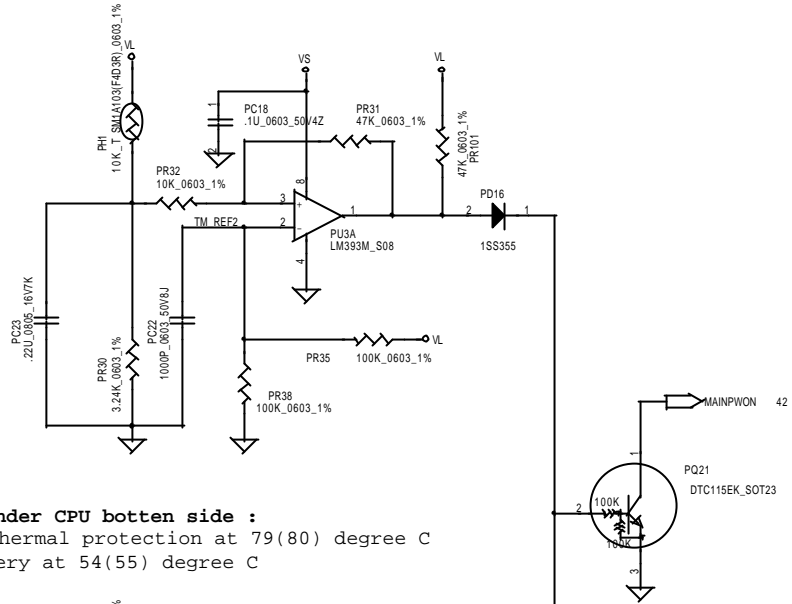
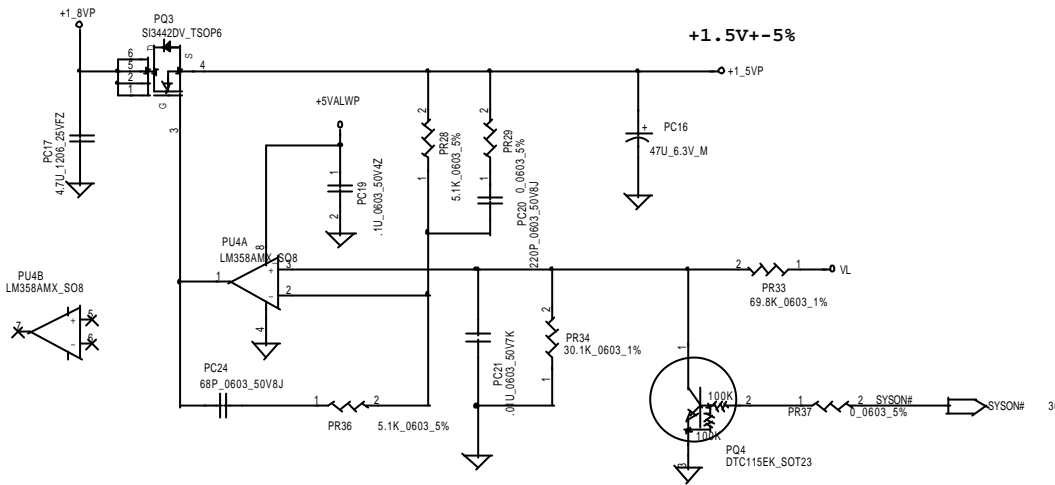
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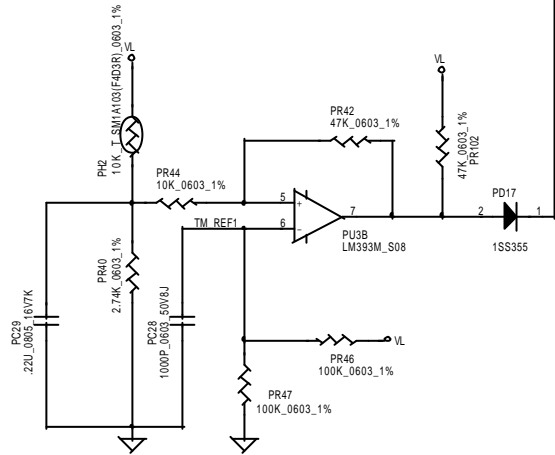
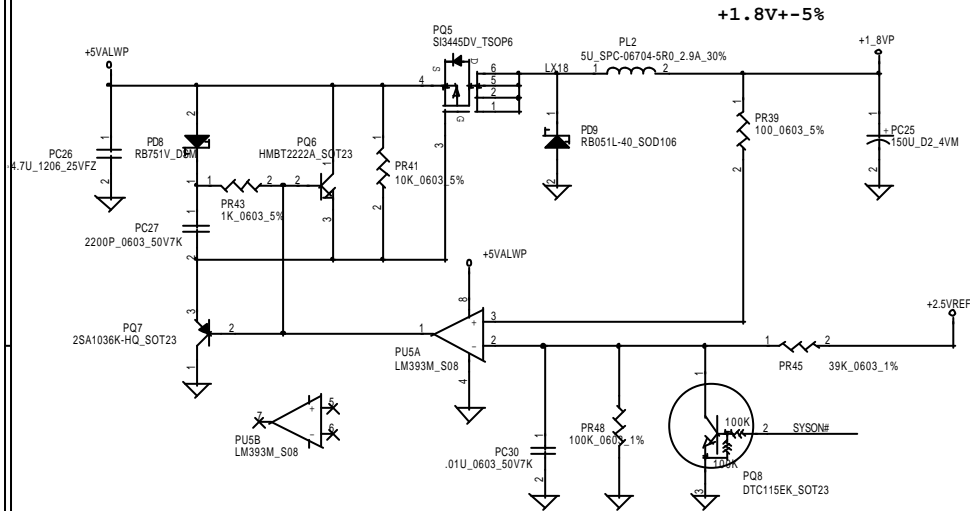
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**PH2 near main Battery CONN :**  
 BAT. thermal protection at 73(74) degree C  
 Recovery at 50(51) degree C



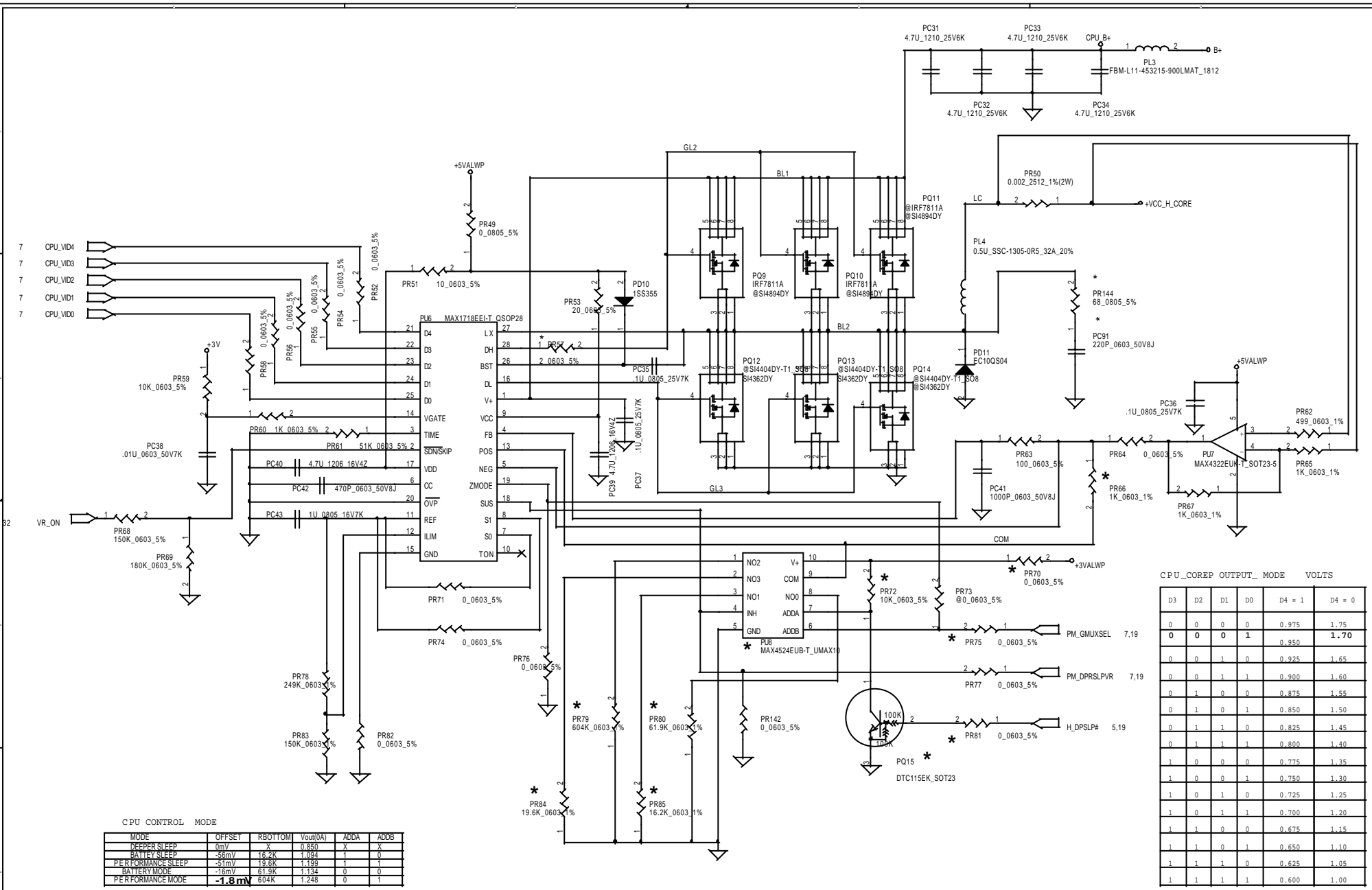
**PH1 under CPU bottom side :**  
 CPU thermal protection at 79(80) degree C  
 Recovery at 54(55) degree C



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CPU CONTROL MODE

MODE	OFFSET	RBO(T)OM	Vout(OA)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTERY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.9K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	-1.8mV	604K	1.248	0	1

CPU\_CORE OUTPUT\_MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	0	0	1	0.950	1.70
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

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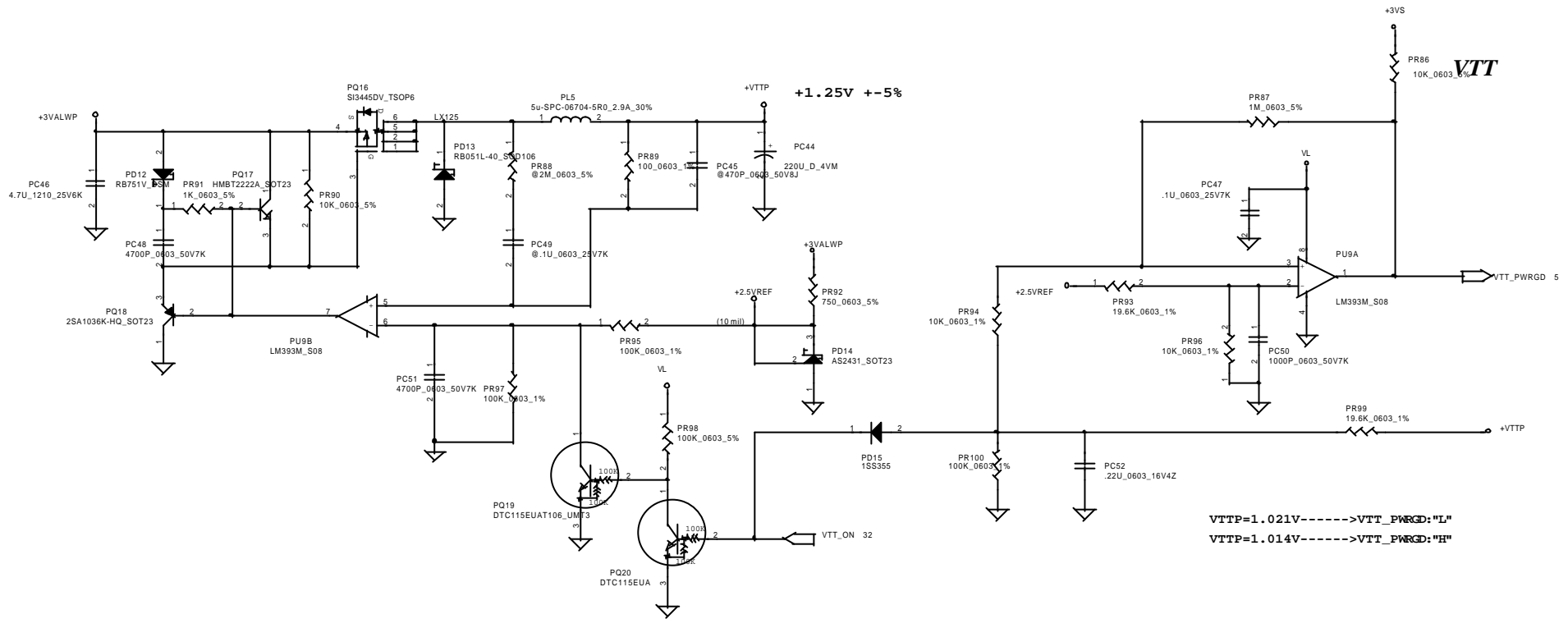
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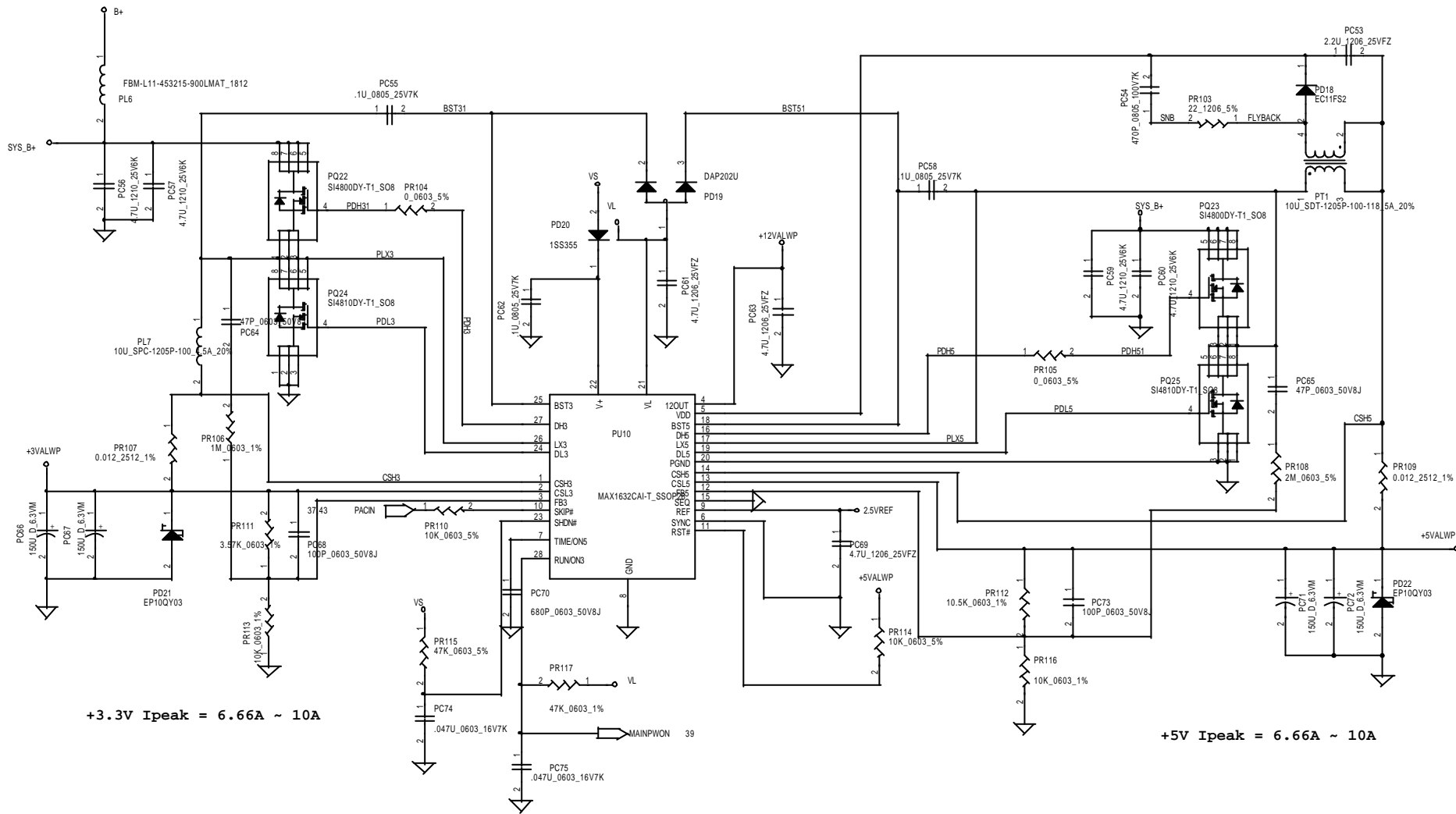
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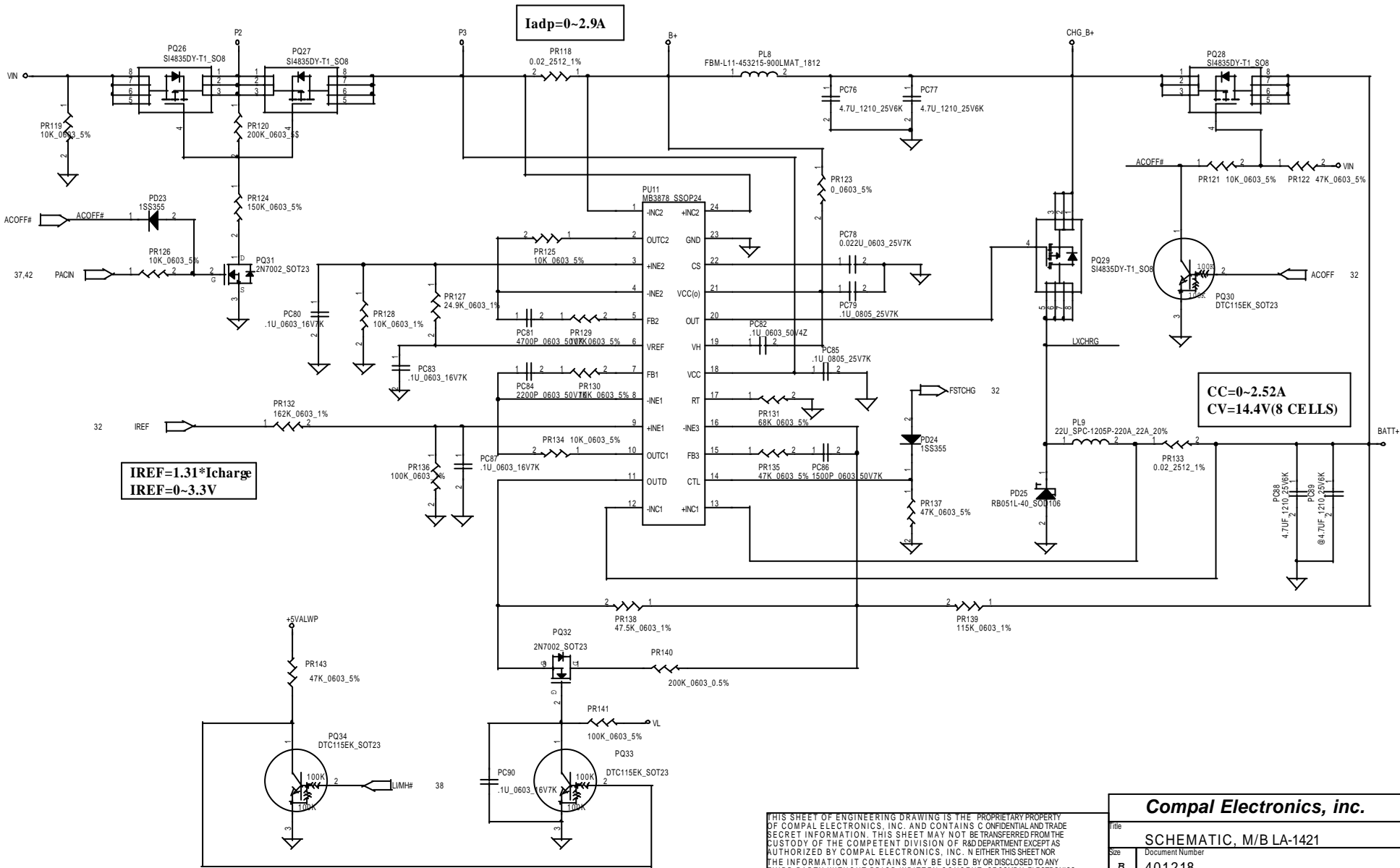


**+3.3V Ipeak = 6.66A ~ 10A**

**+5V Ipeak = 6.66A ~ 10A**

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PIR

Change L35 and L8 size from 0603 to 0805

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REV 0.2

Date	Page	Description
3/29	25	Del R305, R309, D33, D34
	27	Del R64, D9
	33	Q37 added @
	38	Batt SMBus change to EC_SMC1, EC_SMD1
	40	Added PR141
	43	Added PR43, PQ34 and PQ32 change to 2N7002
4/1	24	Del C1, C2, Added C688, C689
4/2	6	C568 added @, C532, C122 change to 220uf Del CF17, CF18, CF19

REV 0.3

Date	Page	Description
4/25	10	C629 C640 change footprint from CAP-A_B_1206_1210_TAN to CAP-D_E_TAN
	28	RP5 RP6 change footprint from 8P4R-0402-NEW to 8P4R
	27&33	Connect DRV0# between JP22 Pin4 and U31 Pin11
	23	Delete R60 Let +3VLAN connect with +3V directly.
4/29	16	Add C690 1000P on net INVT_PWM
	17	Add C691 10P and L47 on net DVOBC_C LKINT#
	28	Delete R17 R451 R9 R450, Change to L50L51 L48 L49
	29	Delete L37 C466 L39 C465 L38 C464 Add C692 C693 C694
	34	Add CP11 C695 C696 C697
4/30	16	Change L35 L8 size from 0603 to 0805
	36	Add C698 C699
5/5	33	Change Board ID from 000 to 001
	28	Change RP5 RP6 Size from 0804 to 1206
	16	Change R339 and R13 from 100Ohm to 00Ohm

REV 1.0

Date	Page	Description
5/30		Update revision code from 0.3 to 1.0 directly

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